

V850E2/MN4 Evaluation Board
Hardware Specifications

March 20, 2010

Rev.1.0

Midas Lab Inc.

Revision History

Revised On	Revision	Chapter	Description
March 20, 2010	1.0		1st edition

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1. INTRODUCTION

The V850E2/MN4 evaluation board is a reference platform for the V850E2/MN4. This board has a range of built-in interfaces, including SRAM, SDRAM, ExBUS, Ethernet, USB 2.0 host and function, SD card, LCD controller, CAN, audio codec, and UART interfaces.

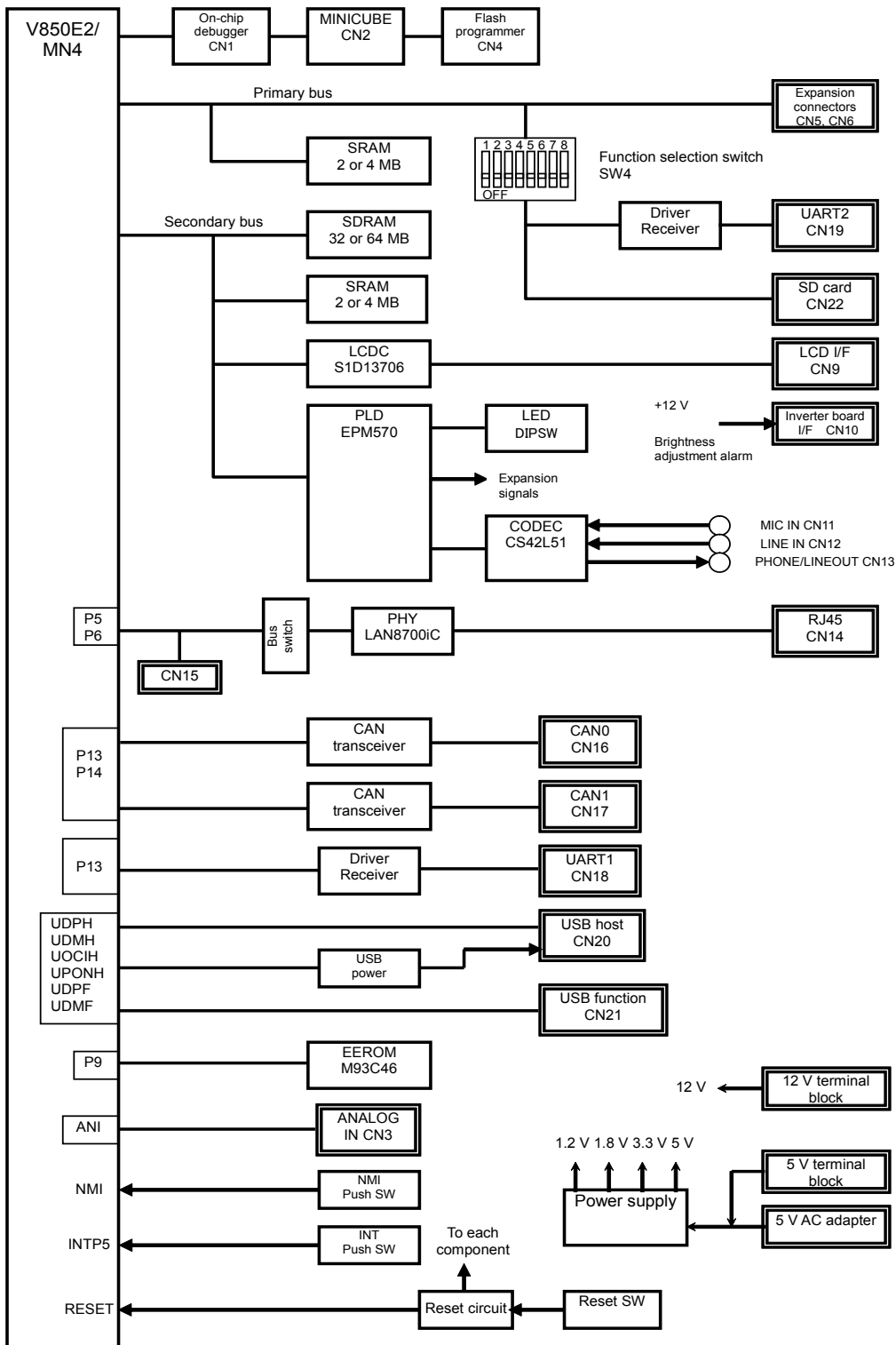
1.1. Numerical Notation

This document uses the numerical notation shown in the table below. For hexadecimal and binary notation, if the number of digits makes the value difficult to read, an underscore (_) is inserted every four digits. Numerical ranges are expressed using a hyphen (-).

Numerical System	Notational Rule	Example
Binary	The number is suffixed with "B".	"10B" represents the decimal number "2".
Decimal	The number is displayed as is.	"10" represents the decimal number "10".
Hexadecimal	The number is suffixed with "H" or prefixed by "0x".	"10H" or "0x10" represents the decimal number "16".

2. FUNCTIONALITY

A diagram of the functional blocks in the V850E2/MN4 evaluation board is shown below.



3. MAJOR FEATURES

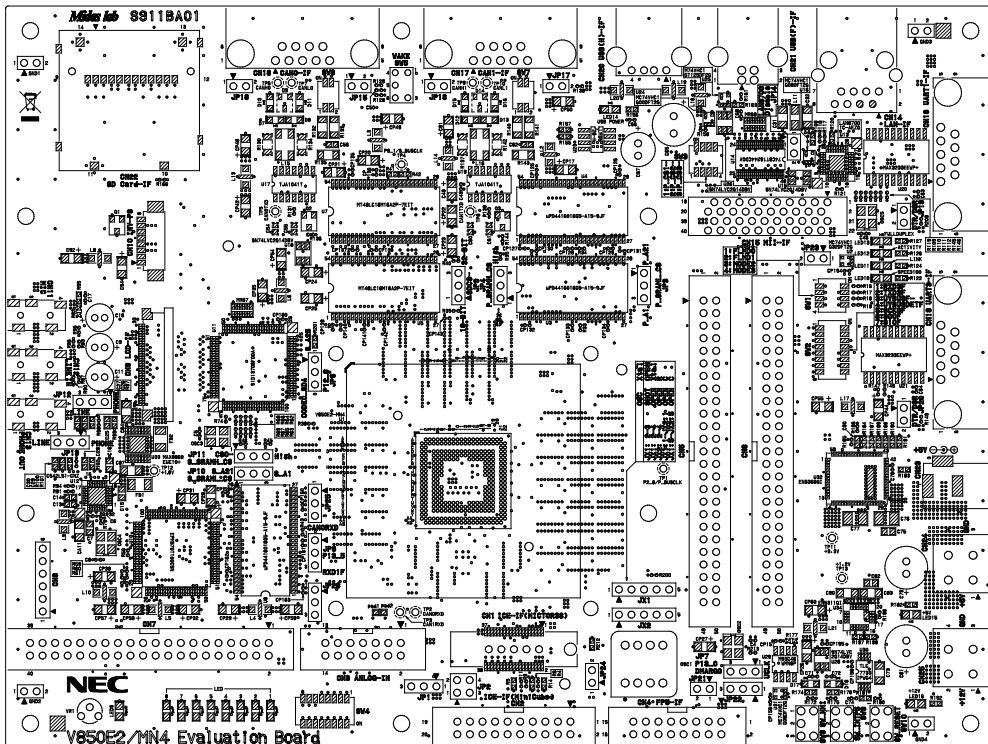
4. BASIC SPECIFICATIONS

Item		General Description	Major Components	
CPU		V850E2/MN4		1
Primary bus memory	SRAM	16-bit bus: 2 MB 32-bit bus: 4 MB Switched by jumper	SRAM: NEC uPD4416016G5	2
Secondary bus memory	SRAM	16-bit bus: 2 MB 32-bit bus: 4 MB Switched by jumper	SRAM: NEC uPD4416016G5	2
	SDRAM	16-bit bus: 32 MB 32-bit bus: 64 MB Switched by jumper	SDRAM: MICRON MT48LC16M16A2P	3
Secondary bus peripherals	PLD	General-purpose DIP switches, general-purpose LEDs, DMA request signals, audio codec control signals, RS232C auxiliary signals, CAN auxiliary signals, SD card control signals	PLD: Altera EPM570T100C5N	1
	LCDC	LCD controller connected via bus LCD panel connector provided	LCDC: Epson S1D13706F00A Connector: Elco 08-6260-033-340-829+	1 1
		Inverter control and brightness adjustment for backlight Inverter error display	Connector: MOLEX 53261-0871	1
CPU ports	USB 2.0 host	V850E2/MN4 USB 2.0 host I/F (A-pin connector)	Connector: AMP 292303-4	1
	USB 2.0 function	V850E2/MN4 USB 2.0 function I/F (B-pin connector)	Connector: AMP 292304-1	1
	UART1, 2	Connected to V850E2/MN4 UART1F and UART3F interfaces	Connector: OMRON XM2C-0912-132	2
			Driver-receiver: Maxim MAX3233	2
	CAN1, 2	Connected to V850E2/MN4 CAN0 and CAN1 interfaces	Connector: OMRON XM3B-0922-132	1
			Transceiver: NXP TJA1041T	1
	CSI	1 Kb EEPROM connected to CSI4	EEROM: ST Micro M93C46	1
	SD card	SD I/F connected to CSI0	Connector: Alps SCDA3A0202	1
Ethernet	10/100 Mbps Ethernet connected to ports P5 and P6 on V850E2/MN4 Connector for connecting PHY board provided	PHY: SMSC LAN8700iC	1	
		Connector: TDK TLA-6T717W	1	
		Connector: AMP 6-5174215-2	1	
ADC	Connected to ANI on V850E2/MN4	Connector: OMRON XG4C-1431	1	
PLD ports	Codec	Audio codec provided Serial control from PLD ports	Codec: CIRRUS LOGIC CS42L51	1
		Connector: Hosiden HSJ1636-01054	3	
Primary bus peripherals	Primary bus expansion	Primary bus expansion connector	Connector: OMRON XG4C-5031	2

Item		General Description	Major Components	
Supplied power	AC adapter power supply or terminal block	+5 V: xxA	Power supply jack HEC0470-01-630 Terminal block: Sato Parts ML-950-2	1 1
	Terminal block	+12 V: xxA	Terminal block: Sato Parts ML-950-2	1
Derived power	+3.3 V	Maximum current: 6 A	EN5366QI (Enpirion)	1
	+1.8 V	Maximum current: 1 A	MAX8869EUE10 (MAXIM)	1
	+1.2 V	Maximum current: 1 A	EN5311QI (Enpirion)	1
MISC	Connectors	Connector for on-chip debugger	Connector: AMP 2-5767004-2	1
		Connector for MINICUBE	Connector: OMRON XG4C-2031	1
		Connector for flash memory programmer	Connector: OMRON XG4C-1631	1
		Connector for PLD programmer	Connector: OMRON XG8V-0631	1
		V850E2/MN4 CPU clock selection	MF-30-1-5	2
		Test pin	Connector: OMRON XG4C-4031	1
	Switches	DIP switch for mode setting	SW: Copal CHS-04TA1	1
		DIP switch for disconnecting common pin signals	SW: Copal CHS-08TA1	1
		DIP switch for selecting SRAM base address of primary bus	SW: Copal CHS-04TA1	1
		General-purpose DIP switch (PLD port)	SW: Copal CHS-08TA1	1
		DIP switch for terminating CAN transmission lines	SW: Copal CHS-02TA1	2
		Switch for waking up CAN	SW: Nikkai G-19AP	1
		Push-button switch for NMI	SW: Fujisoku FP1F-2M-Z	1
		Push-button switch for INT5	SW: Fujisoku FP1F-2M-Z	1
		Toggle switch for reset	SW: Fujisoku FT1F-2M-Z	1
	LEDs	General-purpose LED (PLD port)	LED: Rohm SML-210PTT86	8
		LAN status LED (SPEED100, LINK, ACTIVITY, FULLDUPLEX)	LED: Rohm SML-210PTT86	4
		USB power supply indicator	LED: Rohm SML-210PTT86	1
		Error display on backlight inverter board	LED: Stanley FR1112H	1
		+5 V power supply input indicator	LED: Stanley UB1112H	1
		+12 V power supply input indicator	LED: Stanley UB1112H	1
	VR	For backlight brightness adjustment	VR: Copal RJ-4EW 50 kΩ	1

5. BOARD CONFIGURATION

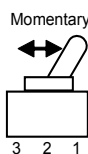
The physical allocation of the main components on the V850E2/MN4 evaluation board is shown in the figure below, followed by a description of each.



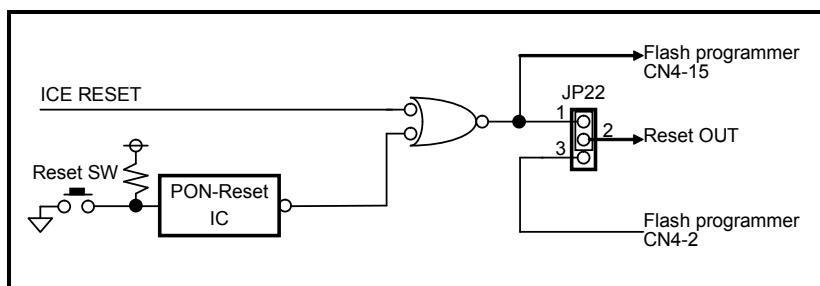
Allocation of Components on V850E2/MN4 Evaluation Board

5.1. Reset Switch (SW10)

This switch is used to reset the system. This is a momentary switch. When the lever is pushed in the opposite direction, the system is reset. When the lever is released, it returns to the original position.

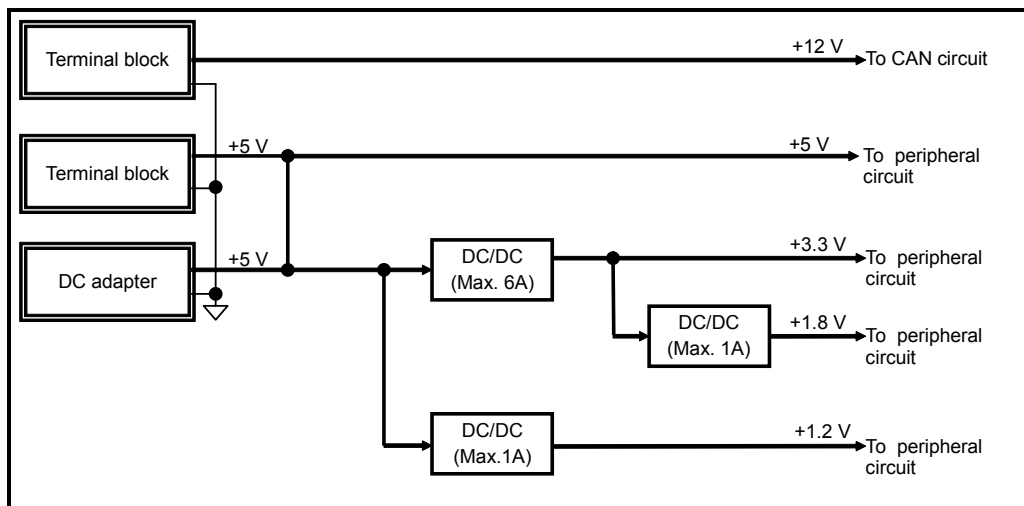


A diagram of the reset circuit is shown below. Jumper pins 1 and 2 of JP22 are shorted by default.

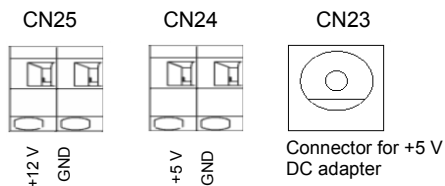


5.2. Power Supply Connectors (CN23, CN24, CN25)

+5 V is supplied from the +5 V DC adapter or +5 V terminal block, and +12 V is supplied from the +12 V terminal block. A diagram of the power supply circuit is shown below.



Do not mistake the +5 V and +12 V terminal blocks.



CN24, CN25

Manufactured by: Sato Parts

Part number: ML-950-2

CN23

Manufactured by: Hosiden

Part number: HEC0470-01-630

DC adapter connector

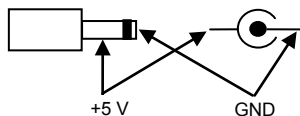
The power supply applied to CN23 has the following specifications:

Voltage: +5 V

Current: (MAX)

Connector: Type A (Φ5.5)

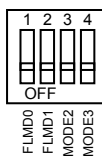
Polarity: See below.



Check that the polarity of the power supply connector is correct.

5.3. Switch 1 (SW1)

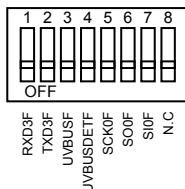
SW1 is used to determine whether the CPU of the V850E2/MN4 operates in flash programming mode or normal mode.



Number	Signal Name	Factory Setting	Description
1	FLMD0	ON	Sets the level of the CPU's FLMD0 pin (ON: Low; OFF: High).
2	FLMD1	ON	Sets the level of the CPU's FLMD1 pin (ON: Low; OFF: High).
3	MODE2	ON	Sets the level of the CPU's MODE2 pin (ON: Low; OFF: High).
4	MODE3	ON	Sets the level of the CPU's MODE3 pin (ON: Low; OFF: High).

5.4. Switch 2 (SW2)

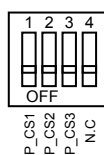
SW2 is used to disconnect the interface circuits connected to multifunction pins on the V850E2/MN4 so that they do not conflict. Each of the contacts on the switch can be set individually. SW2 can be used to prevent signal collision on the board when using the primary bus expansion connectors (CN5 and CN6). For details of the CPU pin connections, see 9.1.



Number	Signal Name	Factory Setting	Description
1	RXD3F	OFF	ON: P4_6 is used as RXD3F. OFF: P4_6 is used as EX_P4_6.
2	TXD3F	OFF	ON: P4_7 is used as TXD3F. OFF: P4_7 is used as EX_P4_7.
3	UVBUSF-	OFF	ON: P4_9 is used as UVBUSF-. OFF: P4_9 is used as EX_P4_9 or P_CS2-.
4	UVBUSDETF	OFF	ON: P4_10 is used as UVBUSDETF. OFF: P4_10 is used as EX_P4_10.
5	SCK0F	OFF	ON: P4_11 is used as SCK0F. OFF: P4_11 is used as EX_P4_11.
6	SO0F	OFF	ON: P4_12 is used as SO0F. OFF: P4_12 is used as EX_P4_12.
7	SI0F	OFF	ON: P4_13 is used as SI0F. OFF: P4_13 is used as EX_P4_13.
8		OFF	Not used

5.5. Switch 3 (SW3)

SW3 is used to select the SRAM base address. The SRAM base address can be selected by using P_CS1, P_CS2, or P_CS3. Note that only one of these contacts can be on at one time. SW3 can also be used to disconnect the SRAM from the bus.

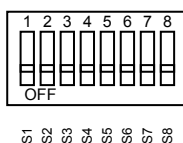


Number	Signal Name	Factory Setting	Description
1	P_CS1	ON	ON: Address space of 0x0200_0000 to 0x03FF_FFFF selected. OFF: Disconnected
2	P_CS2	OFF	ON: Address space of 0x0400_0000 to 0x07FF_FFFF selected. OFF: Disconnected
3	P_CS3	OFF	ON: Address space of 0x0800_0000 to 0x0BFF_FFFF selected. OFF: Disconnected
4		OFF	Not used

5.6. Switch 4 (SW4)

SW4 is a general-purpose DIP switch connected to the PLD. The settings of SW4 can be read by software.

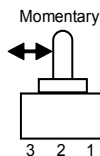
For details of the address and bit configuration of the PLD, see 8.2.7.



Number	Signal Name	Factory Setting	Description
1	S1	OFF	ON: 0 is read; OFF: 1 is read
2	S2	OFF	ON: 0 is read; OFF: 1 is read
3	S3	OFF	ON: 0 is read; OFF: 1 is read
4	S4	OFF	ON: 0 is read; OFF: 1 is read
5	S5	OFF	ON: 0 is read; OFF: 1 is read
6	S6	OFF	ON: 0 is read; OFF: 1 is read
7	S7	OFF	ON: 0 is read; OFF: 1 is read
8	S8	OFF	ON: 0 is read; OFF: 1 is read

5.7. Switch 5 (SW5)

SW5 is a toggle switch used to wake up the CAN. When the lever is in the intermediate position, the CAN is off (a high level is output to CAN_WAKE-). When the lever is pushed to the left or right, the CAN is turned on (a low level is output to CAN_WAKE-). Note that when the lever is pushed to the left, the switch becomes a momentary switch, and the lever returns to the intermediate position when released.



5.8. Switches 6 and 7 (SW6 and SW7)

SW6 and SW7 are used to enable and disable connection of a split terminating resistor on the CAN lines. SW6 is used for CAN0 and SW7 is used for CAN1. CANL and CANH can be set individually, but they must have the same setting.

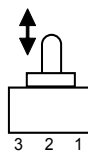


Number	Signal Name	Factory Setting	Description
1	CANH	OFF	ON: Terminated by 62 Ω resistor OFF: Disconnected
2	CANL	OFF	ON: Terminated by 62 Ω resistor OFF: Disconnected

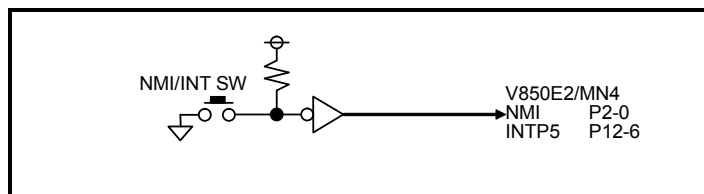
5.9. Switches 8 and 9 (SW8 and SW9)

SW8 and SW9 are push-button switches. When they are pushed, a high level is output to NMI (SW8) or INTP5 (SW9).

These switches are normally off (a low level is output). These switches can be used to manually interrupt operation of the CPU.



A diagram of the NMI/INT circuit is shown below.



5.10. Clock

The V850E2/MN4 uses the clocks shown in the table below. The CPU clock can be selected from the clock generated by the OSC1 oscillator or the clock generated by a crystal resonator by making a jumper setting. When a crystal resonator is used, the required CR settings can also be specified. OSC1 is a socket-type oscillator that can easily be exchanged.

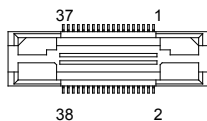
Number	Element	Frequency	Application																		
OSC1	Oscillator	10 MHz	Clock used for V850E2/MN4 CPU Exchangeable socket-type oscillator																		
OSC1'	Resonator	10 MHz	A crystal resonator can be used in place of the oscillator. The CR connections are shown in the table below. <table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th>Setting Location</th> <th>Oscillator</th> <th>Xtal</th> </tr> </thead> <tbody> <tr> <td>JX1:2-3</td> <td>Shorted</td> <td>Open</td> </tr> <tr> <td>JX1:2-4</td> <td>Open</td> <td>Xtal</td> </tr> <tr> <td>JX2:2-4</td> <td>Open</td> <td>R</td> </tr> <tr> <td>JX1:1-JX2:1</td> <td>Open</td> <td>C</td> </tr> <tr> <td>JX1:5-JX2:5</td> <td>Open</td> <td>C</td> </tr> </tbody> </table> <p style="text-align: center;"><u>The oscillator is selected by default.</u></p>	Setting Location	Oscillator	Xtal	JX1:2-3	Shorted	Open	JX1:2-4	Open	Xtal	JX2:2-4	Open	R	JX1:1-JX2:1	Open	C	JX1:5-JX2:5	Open	C
Setting Location	Oscillator	Xtal																			
JX1:2-3	Shorted	Open																			
JX1:2-4	Open	Xtal																			
JX2:2-4	Open	R																			
JX1:1-JX2:1	Open	C																			
JX1:5-JX2:5	Open	C																			
OSC2	Oscillator	48 MHz	Dedicated USB clock (Selected when 1 and 2 on JP7 are shorted) <u>1 and 2 on JP7 are shorted by default.</u>																		
OSC3	Oscillator	50 MHz	Clock for LCD controller IC																		
OSC4	Oscillator	12.288 MHz	Clock for codec IC																		
OSC5	Oscillator	25 MHz	Clock for LAN PHY IC																		

5.11. Connector for Debugger (CN1)

CN1 is used to connect an on-chip debugger.

Pin	Signal	Pin	Signal
1	GND1	2	GND2
3	TCK	4	VCCIO
5	TMS	6	TRST
7	TDI	8	RESET
9	TDO	10	FLMD0
11	MSEO0	12	RDYZ
13	MSEO1	14	EVTO
15	NC1	16	EVTI
17	MCKO	18	NC2
19	NC3	20	NC4
21	MDO0	22	MDO8
23	MDO1	24	MDO9
25	MDO2	26	MDO10
27	MDO3	28	MDO11
29	MDO4	30	MDO12
31	MDO5	32	MDO13
33	MDO6	34	MDO14
35	MDO7	36	MDO15
37	GND3	38	GND4

CN1



Manufactured by: AMP

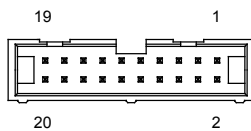
Part number: 2-5767004-2

5.12. Connector for MINICUBE (CN2)

CN2 is used to connect the MINICUBE in-circuit emulator.

Pin	Signal	Pin	Signal
1	GND	2	DCK
3	GND	4	DMS
5	GND	6	DDI
7	GND	8	DRST
9	GND	10	N.C
11	GND	12	RESET
13	GND	14	FLMD0
15	GND	16	TRDY
17	GND	18	DDO
19	GND	20	VDD

CN2

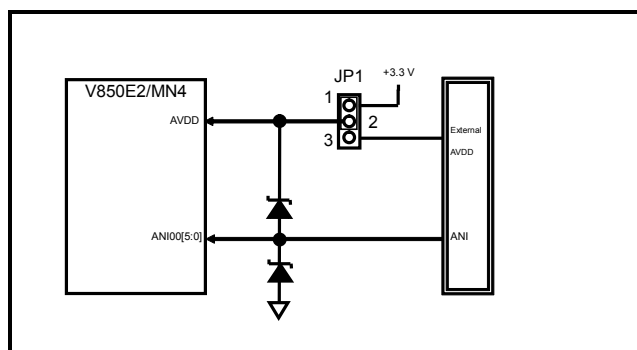


Manufactured by: OMRON

Part number: XG4C-2031

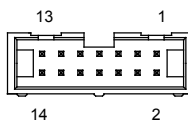
5.13. Connector for Inputting Analog Signals (CN3)

The V850E2/MN4 evaluation board provides an interface for inputting analog signals to the V850E2/MN4’s on-chip 6-channel AD converter with sample & hold circuit. When using the internal power supply (3.3 V), the resolution is 10 bits, but the resolution can be extended to 12 bits by using an external +5 V power supply. The input is clamped to 0 to 3.3 V by using a Schottky diode. Jumper pins 1 and 2 of JP1 are shorted by default, meaning that the 3.3 V internal power supply is selected.



Pin	Signal	Pin	Signal
1	External AVDD input	2	GND
3	ANI00 input	4	GND
5	ANI01 input	6	GND
7	ANI02 input	8	GND
9	ANI03 input	10	GND
11	ANI04 input	12	GND
13	ANI05 input	14	GND

CN3



Manufactured by: OMRON

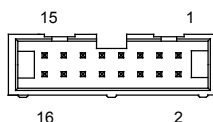
Part number: XG4C-1431

5.14. Connector for Flash Programming Tool (CN4)

CN4 is used to connect a tool for programming the on-chip flash memory of the V850E2/MN4.

Pin	Signal	Pin	Signal
1	GND	2	
3	DDO	4	VDD
5	DDI	6	N.C
7	DCK	8	TRDY
9	DRST	10	N.C
11	N.C	12	DMS
13	N.C	14	FLMD0
15	RESET	16	N.C

CN4



Manufactured by: OMRON

Part number: XG4C-1631

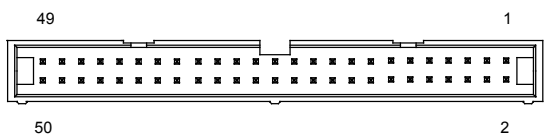
5.15. Connectors for Expanding the Primary Bus (CN5 and CN6)

CN5 and CN6 are used to connect cables to externally expand the primary bus signals of the V850E2/MN4.

The pin assignment is shown in the table below. In the Used For column, P_A0 to P_A23 indicate the address bus and P_D0 to P_D31 indicate the data bus.

Pin Number	Signal Name	Used For	Pin Number	Signal Name	Used For
1	GND		1	GND	
2	EX_P3_0	P_A0	2	EX_P4_0	P_A16
3	EX_P3_1	P_A1	3	EX_P4_1	P_A17
4	EX_P3_2	P_A2	4	EX_P4_2	P_A18
5	EX_P3_3	P_A3	5	EX_P4_3	P_A19
6	GND		6	GND	
7	EX_P3_4	P_A4	7	EX_P4_4	P_A20
8	EX_P3_5	P_A5	8	EX_P4_5	P_A21
9	EX_P3_6	P_A6	9	EX_P4_6	P_A22
10	EX_P3_7	P_A7	10	EX_P4_7	P_A23
11	GND		11	GND	
12	EX_P3_8	P_A8	12	EX_P4_8	P_CS1-
13	EX_P3_9	P_A9	13	EX_P4_9	P_CS2-
14	EX_P3_10	P_A10	14	EX_P4_10	P_CS3-
15	EX_P3_11	P_A11	15	EX_P4_11	P_WAIT
16	GND		16	GND	
17	EX_P3_12	P_A12	17	EX_P4_12	P_HLDAK
18	EX_P3_13	P_A13	18	EX_P4_13	P_HLDRQ
19	EX_P3_14	P_A14	19	N.C	
20	EX_P3_15	P_A15	20	N.C	
21	GND		21	GND	
22	EX_P1_0	P_D16	22	EX_P2_1	P_LLBE-
23	EX_P1_1	P_D17	23	EX_P2_2	P_LUBE-
24	EX_P1_2	P_D18	24	EX_P2_3	P_ULBE-
25	EX_P1_3	P_D19	25	EX_P2_4	P_UUBE-
26	GND		26	GND	
27	EX_P1_4	P_D20	27	EX_P2_5	RD-
28	EX_P1_5	P_D21	28	EX_P2_6	P_BUSCLK
29	EX_P1_6	P_D22	29	EX_P2_7	WR-
30	EX_P1_7	P_D23	30	N.C	
31	GND		31	GND	
32	EX_P1_8	P_D24	32	EX_P0_0	P_D0
33	EX_P1_9	P_D25	33	EX_P0_1	P_D1
34	EX_P1_10	P_D26	34	EX_P0_2	P_D2
35	EX_P1_11	P_D27	35	EX_P0_3	P_D3

Pin Number	Signal Name	Used For	Pin Number	Signal Name	Used For
36	GND		36	GND	
37	EX_P1_12	P_D28	37	EX_P0_4	P_D4
38	EX_P1_13	P_D29	38	EX_P0_5	P_D5
39	EX_P1_14	P_D30	39	EX_P0_6	P_D6
40	EX_P1_15	P_D31	40	EX_P0_7	P_D7
41	GND		41	GND	
42	N.C		42	EX_P0_8	P_D8
43	N.C		43	EX_P0_9	P_D9
44	N.C		44	EX_P0_10	P_D10
45	N.C		45	EX_P0_11	P_D11
46	GND		46	GND	
47	N.C		47	EX_P0_12	P_D12
48	N.C		48	EX_P0_13	P_D13
49	N.C		49	EX_P0_14	P_D14
50	N.C		50	EX_P0_15	P_D15
CN5			CN6		



Manufactured by: OMRON

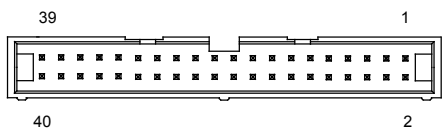
Part number: XG4C-5031

5.16. Connector for Test Pins (CN7)

CN7 is used to connect the test pin signals.

Pin	Signal	Pin	Signal
1	TP7_0	2	TP7_1
3	TP7_2	4	TP7_3
5	GND	6	TP7_4
7	TP7_5	8	TP7_6
9	TP7_7	10	GND
11	TP7_8	12	TP7_9
13	TP7_10	14	TP7_11
15	GND	16	TP7_12
17	TP7_13	18	TP7_14
19	TP7_15	20	GND
21	TP8_0	22	TP8_1
23	TP8_2	24	TP8_3
25	GND	26	TP8_4
27	TP8_5	28	TP8_6
29	TP8_7	30	GND
31	TP8_8	32	TP8_9
33	TP8_10	34	TP8_11
35	GND	36	TP8_12
37	TP8_13	38	TP8_14
39	TP8_15	40	GND

CN7



Manufactured by: OMRON

Part number: XG4C-4031

5.17. Connector for Programming the PLD (CN8)

CN8 is a through-hole connector used to connect the signals for programming the PLD (EPM570T100C5N). The shape of this connector differs from the shape of Altera’s ByteBlaster, so ByteBlaster is connected via a conversion adapter using a JTAG interface.

This connector is used for testing before factory shipment.

Pin	Signal
1	TCK
2	TMS
3	TDI
4	TDO
5	+3.3 V
6	GND

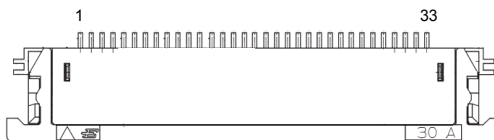
CN8

5.18. Connector for LCD Panel Module Interface (CN9)

CN9 can be used to connect the LCD controller (S1D13706) signals from a TFT color LCD module with a 5.5-inch QVGA screen (NL3224BC35-20).

Pin	Signal	Pin	Signal
1	GND	2	CLK
3	HSYNC	4	VSYNC
5	GND	6	R0
7	R1	8	R2
9	R3	10	R4
11	R5	12	GND
13	G0	14	G1
15	G2	16	G3
17	G4	18	G5
19	GND	20	B0
21	B1	22	B2
23	B3	24	B4
25	B5	26	GND
27	DE	28	VCC
29	VCC	30	DPSH
31	DPSV	32	Q/V
33	GND		

CN9



Manufactured by: KYOCERA ELCO

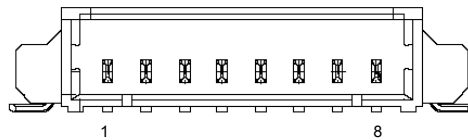
Part number: 08-6260-033-340-829+

5.19. Connector for LCD Panel Backlight (CN10)

CN10 can be used to connect an inverter for controlling the LCD backlight (55PW131).

Pin	Signal
1	VDDDB0
2	VDDDB1
3	GNDDB0
4	GNDDB1
5	BRTC
6	BRT1
7	GNDDB2
8	AM

CN10

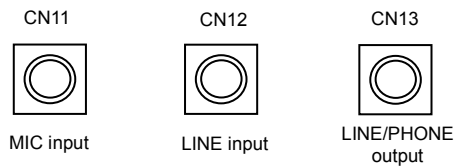


Manufactured by: Molex

Part number: 53261-0871

5.20. Stereo Jack Connectors (CN11, CN12, and CN13)

CN11, CN12, and CN13 are stereo jack connectors used to input and output the audio codec signals.



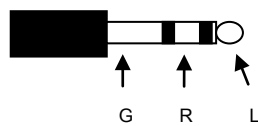
CN11, CN12, and CN13

Manufactured by: Hosiden

Part number: HSJ1636-01054

Adapter:

3.5 mm mini plug

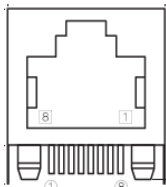


5.21. LAN Connector (CN14)

CN14 is an RJ45 connector for a 10BASE-T/100BASE-T LAN. CN14 has a built-in pulse transformer.

Pin	Signal
1	TD+
2	TD-
3	RD+
4	CT1
5	CT2
6	RD-
7	CT3
8	CT4

CN14



Manufactured by: TDK

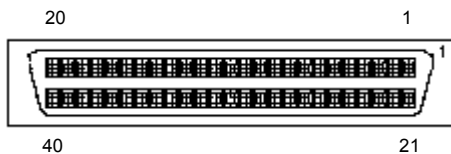
Part number: TLA-6T717W

5.22. PHY Daughter Card Connector (CN15)

CN15 is a daughter card connector that enables PHY chips other than the mounted LAN8700iC chip to be used. When using CN15, the mounted chip must be disconnected from the bus by using JP14. For details, see **8.5**.

Pin	Signal	Pin	Signal
1	+5 V[3]	21	+5 V[2]
2	MDIO	22	COMMON[18]
3	MDC	23	COMMON[17]
4	RXD3	24	COMMON[16]
5	RXD2	25	COMMON[15]
6	RXD1	26	COMMON[14]
7	RXD0	27	COMMON[13]
8	RX_DV	28	COMMON[12]
9	RX_CLK	29	COMMON[11]
10	RX_ER	30	COMMON[10]
11	TX_ER	31	COMMON[9]
12	TX_CLK	32	COMMON[8]
13	TX_EN	33	COMMON[7]
14	TXD0	34	COMMON[6]
15	TXD1	35	COMMON[5]
16	TXD2	36	COMMON[4]
17	TXD3	37	COMMON[3]
18	COL	38	COMMON[2]
19	CRS	39	COMMON[1]
20	+5 V[4]	40	+5 V[1]

CN15



Manufactured by: AMP/Tyco

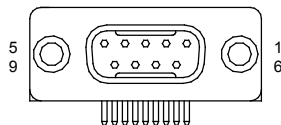
Part number: 6-5174215-2

5.23. CAN Connectors (CN16 and CN17)

CN16 and CN17 are used to connect the interfaces for the CPU's built-in CAN device controllers.

Pin	Signal
1	
2	CANL
3	GND
4	
5	
6	
7	CANH
8	
9	

CN16/CN17



Manufactured by: OMRON

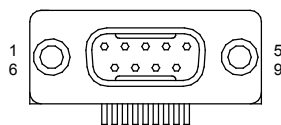
Part number: XM3B-0922-132

5.24. UART Connectors (CN18 and CN19)

CN18 and CN19 are used to connect the interfaces for the CPU's built-in UART device controllers.

Pin	Signal
1	DCD
2	RX
3	TX
4	DTR
5	GND
6	DSR
7	RTS
8	CTS
9	RI

CN18/CN19



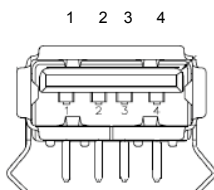
Manufactured by: OMRON
 Part number: XM2C-0912-132

5.25. USB Host Connector (CN20)

CN20 is used to connect the interface for the CPU's built-in USB host controller. CN20 is a standard A receptacle.

Pin	Signal
1	VBus
2	-Data
3	+Data
4	GND

CN20



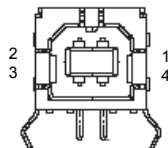
Manufactured by: AMP
 Part number: 292303-4

5.26. USB Function Connector (CN21)

CN21 is used to connect the interface for the CPU's built-in USB function controller. CN21 is a standard B receptacle.

Pin	Signal
1	VBus
2	-Data
3	+Data
4	GND

CN21

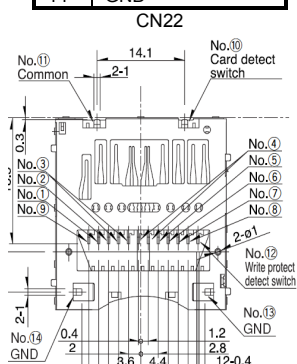


Manufactured by: AMP
 Part number: 292304-1

5.27. SD Card Connector (CN22)

CN22 is used to connect an SD card interface.

Pin	Signal
1	CD/DAT3 (CS-)
2	CMD (Datain)
3	VSS
4	VDD
5	CLK (CLK)
6	VSS
7	DATA0 (Dataout)
8	DAT1
9	DAT2
10	CD
11	COM
12	WP
13	GND
14	GND



Manufactured by: ALPS

Part number: SCDA3A0202

5.28. AVDD Selection Jumper (JP1)

JP1 is used to select whether AVDD is supplied from the microcontroller chip (1 and 2 shorted) or from an external power supply via the CN3 connector (2 and 3 shorted). If an internal power supply is selected, +3.3 V is supplied as AVDD. If an external power supply is selected, up to +5 V can be supplied.

1 and 2 are shorted by default.

5.29. Jumper (JP2)

JP2 is used to specify the signal to be connected to pin 14 of the MINICUBE connector (CN2). To connect the FLMD0 signal, short 1 and 2. To connect the EVTOZ signal, short 3 and 4.

1 and 2 are shorted by default, specifying the FLMD0 signal.

5.30. Primary SRAM Bus Width Selection Jumpers (JP3 and JP4)

JP3 and JP4 are used to select the width of the bus used for the primary SRAM. To use a 32-bit bus, short 1 and 2. To use a 16-bit bus, short 2 and 3. JP3 and JP4 must both have the same settings.

1 and 2 are shorted by default, selecting a 32-bit bus.

5.31. Jumper for Selecting the Function of P12-8 (JP6)

JP6 is used to select the function of pin 8 of port 12 in the CPU. To use this pin as S1_HA25, short 1 and 2. To use this pin as SDA for the codec, short 2 and 3.

1 and 2 are shorted by default, selecting S1_HA25.

5.32. Jumper for Selecting the Function of P13-0 (JP7)

JP7 is used to select the function of pin 0 of port 13 in the CPU. To use this pin as the USB clock input (48 MHz), short 1 and 2. To use this pin as the S_DMARQ0 input, short 2 and 3.

1 and 2 are shorted by default, selecting the USB clock input.

5.33. Jumper for Selecting the Function of P13-5 (JP8)

JP8 is used to select the function of pin 5 of port 13. To use this pin as CAN0RXD, short 1 and 2. To use this pin as RXD1F, short 2 and 3.

1 and 2 are shorted by default, selecting CAN0RXD.

5.34. SDRAM Bus Width Selection Jumper (JP9)

JP9 is used to select the width of the SDRAM bus. To use a 16-bit bus, short 1 and 2. To use a 32-bit bus, short 2 and 3.

1 and 2 are shorted by default, selecting a 16-bit bus.

5.35. Secondary SRAM Bus Width Selection Jumpers (JP10 and JP11)

JP10 and JP11 are used to select the width of the bus used for the secondary SRAM. To use a 32-bit bus, short 1 and 2. To use a 16-bit bus, short 2 and 3. JP10 and JP11 must both have the same settings.

1 and 2 are shorted by default, selecting a 32-bit bus.

5.36. PHONE/LINE Output Selection Jumpers (JP12 and JP13)

JP12 and JP13 are used to select between PHONE output and LINE output. To select PHONE output for the right side (JP12) or the left side (JP13), short 1 and 2. To select LINE output, short 2 and 3. JP12 and JP13 must both have the same settings.

1 and 2 are shorted by default, selecting PHONE output.

5.37. LAN8700iC Bus Selection Jumper (JP14)

JP14 is used to select whether to disconnect LAN8700iC from the bus on the board or not. To disconnect LAN8700iC from the bus, short JP14. To keep LAN8700iC connected to the bus, leave

JP14 open.

JP14 is left open by default, enabling the use of LAN8700iC.

5.38. Ground Connection Selection Jumpers (JP15, JP16, JP17, and JP18)

These jumpers are used to select whether to ground pins 5 and 6 of the CAN connectors. To ground pins 5 and 6, short these jumpers.

JP15 corresponds to pin 5 of CN16, JP16 corresponds to pin 6 of CN16, JP17 corresponds to pin 5 of CN17, and JP18 corresponds to pin 6 of CN17.

JP15 and JP17 are shorted and JP16 and JP18 are left open by default.

5.39. DSR-DTR Loopback Selection Jumpers (JP19 and JP20)

JP19 and JP20 are used to select whether to loop back the DSR and DTR signals in UART connectors CN18 and CN19. To loop back the signals, short these jumpers.

JP19 is for CN18 and JP20 is for CN19.

Both JP19 and JP20 are shorted by default.

5.40. Jumper for Selecting Connection of DDO and DDI on Flash Programmer (JP21)

To connect DDO to DDI and use them as a bidirectional signal, short this jumper.

JP21 is left open by default, meaning that DDO and DDI are used independently.

5.41. Reset Signal Selection Jumper (JP22)

JP22 is used to select the CPU reset signal. JP22 is usually used with 1 and 2 shorted. To select the reset signal output from the flash programmer as the CPU reset signal, short 2 and 3.

1 and 2 are shorted by default.

5.42. Jumper (JP23)

Short this jumper to enable FLMD0.

JP23 is shorted by default.

5.43. TDO Pull-up Selection Jumper (JP24)

Short this jumper to pull up the TDO pin on the on-board debugger connector.

JP24 is shorted by default, meaning that the TDO pin is pulled up.

6. HARDWARE REFERENCE

This section describes the hardware specifications of the V850E2/MN4 evaluation board.

6.1. Allocation of Memory and Peripherals

The memory and peripherals on the evaluation board are allocated to the following areas:

0xFFFF_FFFF 0xFFFF_5000	On-chip peripheral I/O area	44 KB
0xFFFF_4FFF 0xFF84_0000	Reserved area	8 MB
0xFF83_FFFF 0xFF40_0000	On-chip peripheral I/O area	4 MB
0xFF3F_FFFF 0xFEE0_0000	Reserved area	6 MB
0xFEDF_FFFF 0xFEDF_0000	RAM 1 area	64 KB
0xFEDE_FFFF 0xFEC0_0000	Reserved area	2 MB
0xFEBC_FFFF 0xFEBF_0000	RAM 2 area	64 KB
0xFEBC_FFFF 0xFA00_0000	Reserved area	76 MB
0xF9FF_FFFF 0xF993_3400	Reserved area	7 MB
0xF993_33FF 0xF993_3000	On-chip peripheral I/O area	1 KB
0xF993_2FFF 0xF993_2400	Reserved area	3 KB
0xF993_23FF 0xF993_0000	On-chip peripheral I/O area	9 KB
0xF992_FFFF 0xF990_1400	Reserved area	187 KB
0xF990_13FF 0xF990_0000	On-chip peripheral I/O area	5 KB
0xF98F_FFFF 0xF981_0000	Reserved area	960 KB
0xF980_FFFF 0xF980_0000	EX-RAM area	64 KB
0xF97F_FFFF 0xF960_0000	Secondary CS3 area Not used	2 MB
0xF95F_FFFF 0xF940_0000	Secondary CS2 area Used for ports in LCDC	2 MB
0xF93F_FFFF 0xF900_0000	Secondary CS1 area Used for ports in PLD	4 MB
0xF8FF_FFFF 0xF800_0000	Secondary CS0 area Used for external SRAM <3>	16 MB (4 MB)
0xF7FF_FFFF 0xF000_0000	Secondary SDRAM CS area Used for external SDRAM <2>	128 MB (64 MB)
0x0FFF_FFFF 0x0C00_0000	Reserved area	64 MB
0x0BFF_FFFF 0x0800_0000	Primary CS3 area Used for external SRAM <1>	64 MB (4 MB)
0x07FF_FFFF 0x0400_0000	Primary CS2 area Used for external SRAM <1>	64 MB (4 MB)
0x03FF_FFFF 0x0200_0000	Primary CS1 area Used for external SRAM <1>	32 MB (4 MB)
0x01FF_FFFF 0x0020_0000	Reserved area	30 MB
0x001F_FFFF 0x0000_0000	On-chip flash memory area	2 MB

Map of memory and I/O peripherals

Figures in parentheses refer to the amount of area used. The remaining capacity is image area.

<1> The capacity of the external SRAM is 2 MB when a 16-bit bus is used and 4 MB when a 32-bit bus is used. External SRAM can only be allocated to one area: primary CS1 area, primary CS2 area, or primary CS3 area.

<2> The capacity of the external SDRAM is 32 MB when a 16-bit bus is used and 64 MB when a 32-bit bus is used.

<3> The capacity of the external SRAM is 2 MB when a 16-bit bus is used and 4 MB when a 32-bit bus is used.

Primary CS1 area (SRAM): 0x0200_0000 to 0x03FF_FFFF (32 MB)

Primary CS2 area (SRAM): 0x0400_0000 to 0x07FF_FFFF (64 MB)

Primary CS3 area (SRAM): 0x0800_0000 to 0x0BFF_FFFF (64 MB)

SRAM can only be allocated to one area: primary CS1 area, primary CS2 area, or primary CS3 area. The actual capacity of the SRAM differs depending on the width of the bus. When using a 16-bit bus, the capacity of the SRAM is 2 MB; when using a 32-bit bus, the capacity of the SRAM is 4 MB. The space that remains after subtracting the actual capacity of the SRAM is SRAM image space.

Unused areas can be used for external expansion.

Secondary SDRAM CS area (SDRAM): 0xF000_0000 to 0xF7FF_FFFF (128 MB)

SDRAM is allocated to this area. The actual capacity of the SDRAM differs depending on the width of the bus. When using a 16-bit bus, the capacity of the SDRAM is 32 MB; when using a 32-bit bus, the capacity of the SDRAM is 64 MB. The space that remains after subtracting the actual capacity of the SDRAM is SDRAM image space.

Secondary CS0 area (SRAM): 0xF800_0000 to 0xF8FF_FFFF (16 MB)

SRAM is allocated to this area. The actual capacity of the SRAM differs depending on the width of the bus. When using a 16-bit bus, the capacity of the SRAM is 2 MB; when using a 32-bit bus, the capacity of the SRAM is 4 MB. The space that remains after subtracting the actual capacity of the SRAM is SRAM image space.

Secondary CS1 area (PLD): 0xF900_0000 to 0xF93F_FFFF (4 MB)

The I/O ports of the PLD are allocated to this area. The actual space used is 0xF900_0000 to 0xF900_001F. The remaining space is I/O port image space.

Secondary CS2 area (LCDC): 0xF940_0000 to 0xF95F_FFFF (2 MB)

The I/O ports of the LCDC are allocated to this area. The actual space used is 0xF940_0000 to 0xF941_FFFF. The remaining space is I/O port image space.

Secondary CS3 area (not used)

This area is reserved for the SDRAM CS, and therefore cannot be used.

7. MEMORY

7.1. SRAM

A 16 Mb (1 M × 16 bits) SRAM is assigned to each of the primary and secondary CS areas. The base address of the primary CS area SRAM can be changed, as shown in the table below.

Selection of Address Space According to DIPSW (SW3[4:1]) Settings

SW3[4]	SW3[3]	SW3[2]	SW3[1]	16-Bit Bus	32-Bit Bus
x	OFF	OFF	ON	0x0200_0000 0x021F_FFFF	0x0200_0000 0x023F_FFFF
x	OFF	ON	OFF	0x0400_0000 0x041F_FFFF	0x0400_0000 0x043F_FFFF
x	ON	OFF	OFF	0x0800_0000 0x081F_FFFF	0x0800_0000 0x083F_FFFF
x	OFF	OFF	OFF	Disable	

x: don't care

Only one of SW3[1] to SW3[3] can be on at the same time.

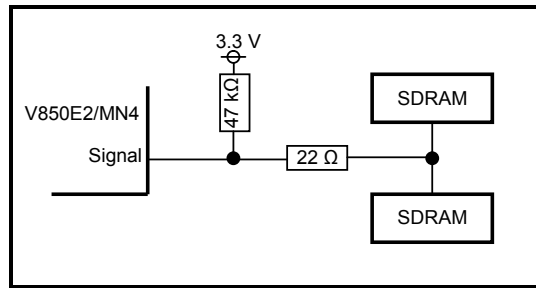
The width of the bus used for each of the SRAMs can be specified separately. The specifiable bus widths are 16 bits and 32 bits. When 16-bit access is selected, the capacity of the SRAM is 2 MB; when 32-bit access is selected, the capacity of the SRAM is 4 MB. The mounted SRAM is either uPD4416016G5-A15-9JF from NEC or CY7C1061DV33-10ZSXI from Cypress.

7.2. SDRAM

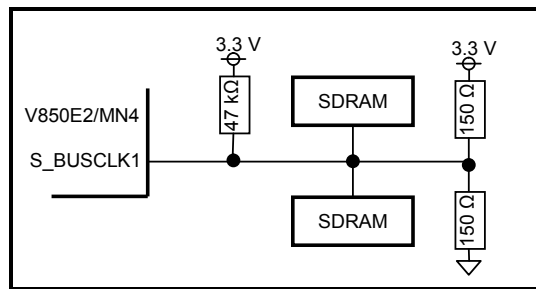
Three 512 Mb (4 M × 16 bits × 4 banks) SDRAMs are mounted on the evaluation board. Note, however, that when using a 16-bit bus, only one SDRAM can be used, and when using a 32-bit bus, only two SDRAMs can be used. Consequently, the actual usable memory capacity when using a 16-bit bus is 32 MB, and 64 MB when using a 32-bit bus. The mounted SDRAM is MT48LC16M16A2P-7EIT from Micron.

	16-Bit Bus	32-Bit Bus
SDRAM space	0xF000_0000 0xF1FF_FFFF	0xF000_0000 0xF3FF_FFFF

The wiring topology for each of the signal groups is shown in the diagrams below.



Address, data, clock, and command signals



S_BUSCLK1 signal

8. I/O DEVICES

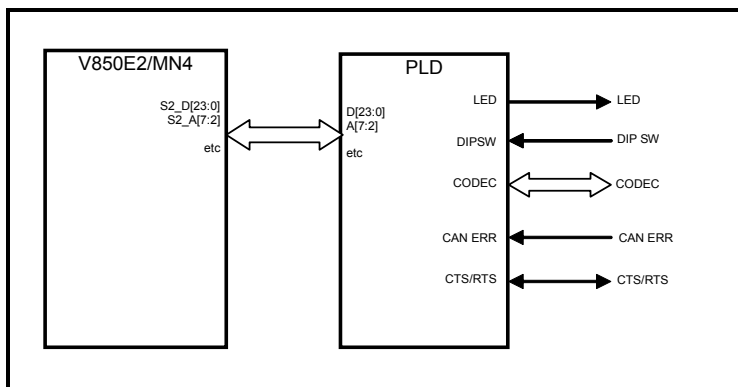
8.1. List of I/O Devices

The I/O devices connected to the bus are shown in the table below.

Address	Device
0xF900_0000 to 0xF900_001F	PLD registers
0xF940_0000 to 0xF940_00B3	LCD controller control registers
0xF942_0000 to 0xF943_FFFF	LCD controller display memory

8.2. PLD (0xF900_0000 to 0xF900_001F)

The PLD is connected to the secondary bus of the V850E2/MN4 and is used as an interface for the audio codec control signals, CAN and UART auxiliary signals, general-purpose LED signals, general-purpose DIP switch signals, and SD card auxiliary signals.



The ports in the PLD are assigned to the secondary CS1 area. Up to 24 data signals (D0 to D23) can be used. The PLD must be accessed using 32-bit access.

The registers in the PLD are described in detail below.

8.2.1. REG0 PLAY_D (0xF900_0000)

Bit	After Reset	Name	R/W	Description
23		DI(23)	WO	Left channel and right channel playback data
22		DI(22)	WO	
21		DI(21)	WO	When DMA is used: Playback data for either the left or right channel is written when the first DMAREQ0 signal is received (active low).
20		DI(20)	WO	
19		DI(19)	WO	
18		DI(18)	WO	
17		DI(17)	WO	When DMA is not used: Playback data for either the left or right channel is written when PLAY_READY is set (1) after PLAY_RUN is set (1).
16		DI(16)	WO	
15		DI(15)	WO	
14		DI(14)	WO	
13		DI(13)	WO	Monaural playback The playback data of the channel used for playback is written. 000000H is written to the channel not used for playback.
12		DI(12)	WO	
11		DI(11)	WO	
10		DI(10)	WO	
9		DI(9)	WO	Playback data is played back from the channels in the order of Lch, Rch, Lch, Rch...after the data is written at the first DMAREQ0 or when PLAY_READY is set (1). A 6-stage FIFO buffer is used for buffering the data.
8		DI(8)	WO	
7		DI(7)	WO	
6		DI(6)	WO	
5		DI(5)	WO	
4		DI(4)	WO	
3		DI(3)	WO	
2		DI(2)	WO	
1		DI(1)	WO	
0		DI(0)	WO	

8.2.2. REG1 PLAY_C (0xF900_0004)

Bit	After Reset	Name	R/W	Description
23			RO	Not used.
22				
21				
20				
19				
18				
17				
16				
15				
14				
13				
12				
11				
10				
9				
8				
7				
6				
5	0	PLAY_UDF	RO	1: An underflow has occurred. This bit is set (1) when the playback data for the left or right channel could not be written in time to be read. This bit is automatically cleared (0) when playback starts.
4	0	DI_INT	RO	Not used.
3	0	PLAY	W/R	1: Start playback. 0: Stop playback.
2	0	PLAY_DMAENB	W/R	1: Use DMAREQ0. 0: Do not use DMAREQ0.
1	0	PLAY_RUN	RO	1: Playback is in progress.
0	0	PLAY_READY	RO	1: Playback data can be written. 0: Playback data cannot be written.

8.2.3. REG2 REC_D (0xF900_0008)

Bit	After Reset	Name	R/W	Description
23		DO(23)	RO	Data to be recorded from the left and right channels.
22		DO(22)	RO	
21		DO(21)	RO	When DMA is used: Data from either the left or right channel is read when the first DMAREQ1 signal is received (active low).
20		DO(20)	RO	
19		DO(19)	RO	When DMA is not used: Data from either the left or right channel is read when REC_READY is set (1) after REC_RUN is set (1).
18		DO(18)	RO	
17		DO(17)	RO	MIC recording When recording from a microphone, only the data from the left channel is valid. The data from the right channel is undefined.
16		DO(16)	RO	
15		DO(15)	RO	Data is recorded from the channels in the order of Lch, Rch, Lch, Rch...after the data is read at the first DMAREQ1 or when REC_READY is set (1).
14		DO(14)	RO	
13		DO(13)	RO	A 6-stage FIFO buffer is used for buffering the data.
12		DO(12)	RO	
11		DO(11)	RO	
10		DO(10)	RO	
9		DO(9)	RO	
8		DO(8)	RO	
7		DO(7)	RO	
6		DO(6)	RO	
5		DO(5)	RO	
4		DO(4)	RO	
3		DO(3)	RO	
2		DO(2)	RO	
1		DO(1)	RO	
0		DO(0)	RO	

8.2.4. REG3 REC_C (0xF900_000C)

Bit	After Reset	Name	R/W	Description
23			RO	Not used.
22				
21				
20				
19				
18				
17				
16				
15				
14				
13				
12				
11				
10				
9				
8				
7				
6				
5	0	REC_OVF	RO	1: An overflow has occurred. This bit is set (1) when the data to be recorded from the left or right channel could not be read before the next data was written. This bit is automatically cleared (0) when recording starts.
4		DO_INT	RO	Not used.
3	0	REC	W/R	1: Start recording. 0: Stop recording.
2	0	REC_DMAENB	W/R	1: Use DMAREQ1. 0: Do not use DMAREQ1.
1	0	REC_RUN	RO	1: Recording is in progress.
0	0	REC_READY	RO	1: Data to be recorded can be read. 0: Data to be recorded cannot be read.

8.2.5. REG4 (0xF900_0010)

Not used.

8.2.6. REG5 RSV (0xF900_0014)

Bit	After Reset	Name	R/W	Description
23				
22				
21				
20				
19				
18				
17				
16				
15				
14				
13				
12			RO	Not used.
11				
10				
9				
8				
7				
6				
5				
4				
3				
2				
1	0	CODEC_nRESET	W/R	0: Execute a hardware reset on the codec. 1: Set the codec to operating mode.
0	0	AD0	W/R	0: Make the signal low (I2C mode). 1: Make the signal high (SPI mode). This bit must be set to 0 (I2C mode).

8.2.7. REG6 MISC (0xF900_0018)

Bit	After Reset	Name	R/W	Description
23				
22				
21				
20				
19				
18				
17			RO	Not used.
16				
15				
14				
13				
12				
11		SD_nWP	RO	Input ports
10		SD_nCD	RO	
9		CTS3F	RO	
8		CTS1F	RO	
7		SW(7)	RO	Input ports (switches) CPLD internal pull-up resistors specified. Weak pull-up resistor on
6		SW(6)	RO	
5		SW(5)	RO	
4		SW(4)	RO	
3		SW(3)	RO	
2		SW(2)	RO	
1		SW(1)	RO	
0		SW(0)	RO	

8.2.8. REG7 (0xF900_001C)

Bit	After Reset	Name	R/W	Description
23		TP1	W/R	Spare pin
22			RO	Not used.
21				
20				
19				
18			RO	Not used.
17				
16				

15				
14				
13	0	CAN1EN	W/R	Output ports
12	0	CAN0EN	W/R	
11	1	nCAN1STB	W/R	
10	1	nCAN0STB	W/R	
9	0	RTS3F	W/R	
8	0	RTS1F	W/R	Output ports (LED indicators) The LEDs turn on when 0 is written.
7	0	LED(7)	W/R	
6	0	LED(6)	W/R	
5	0	LED(5)	W/R	
4	0	LED(4)	W/R	
3	0	LED(3)	W/R	
2	0	LED(2)	W/R	
1	0	LED(1)	W/R	
0	0	LED(0)	W/R	

8.3. Port for Reading SW4 (0xF900_0018)

SW4 is a general-purpose 8-bit switch that can be read by using software.

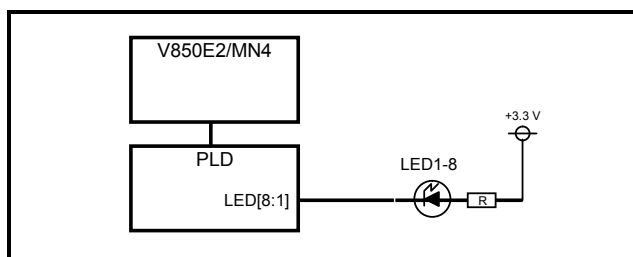
For details of SW4, see 8.2.7 in the PLD register descriptions or 5.6 Switch 4 (SW4).

8.4. Ports for Outputting LED Indication (0xF900_001C)

The evaluation board includes eight LEDs that can be controlled by software, via PLD ports.

Writing 0 to a bit turns on the corresponding LED.

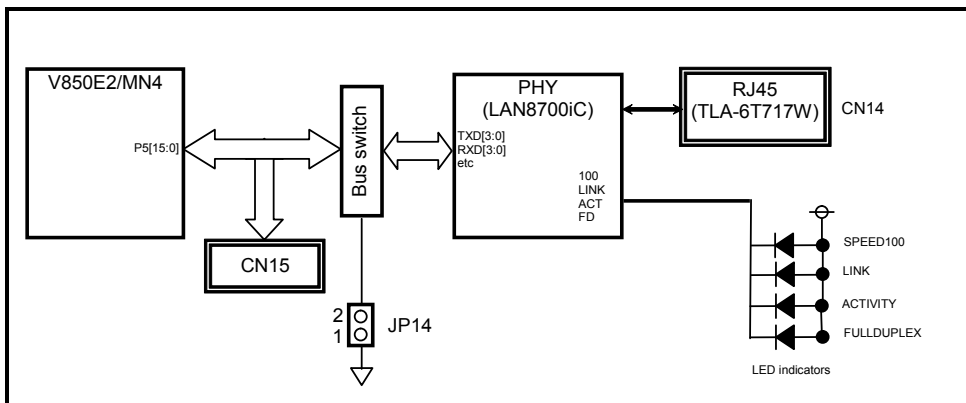
For details of the bit positions, see 8.2.8 in the PLD register descriptions.



8.5. LAN-PHY

This is an Ethernet interface. The V850E2/MN4 interfaces with an Ethernet LAN via this PHY (LAN8700iC). The RJ45 connector has a built-in pulse transformer.

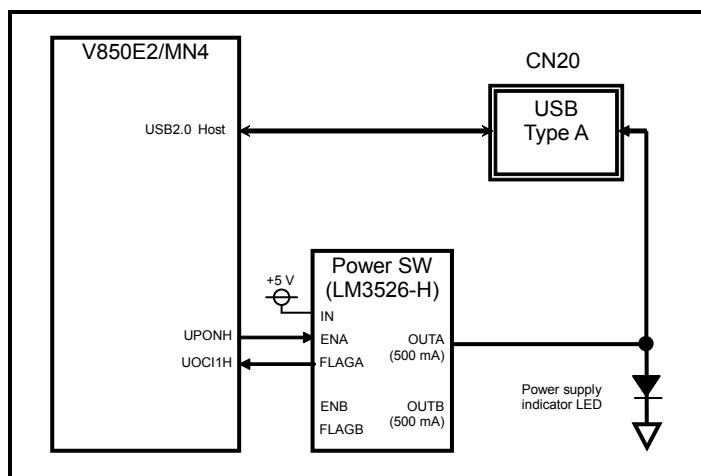
The V850E2/MN4 and PHY (LAN8700iC) are connecting using a bus switch IC, so the PHY (LAN8700iC) can be disconnected from the bus on the board by shorting JP14 and a board with a built-in PHY/RJ45 can be connected separately to CN15.



8.6. USB 2.0 Host

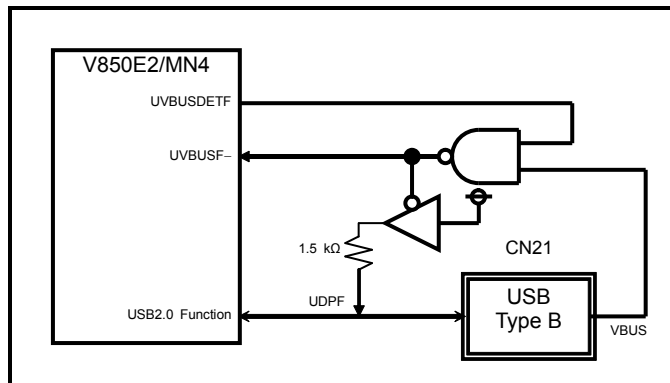
A USB 2.0 host device can interface with the V850E2/MN4 by using the USB host interface incorporated in the V850E2/MN4 chip.

Power can be supplied to USB 2.0 host device via the USB bus. When power is being supplied to the connected USB host device, the power supply indicator (LED) turns on.



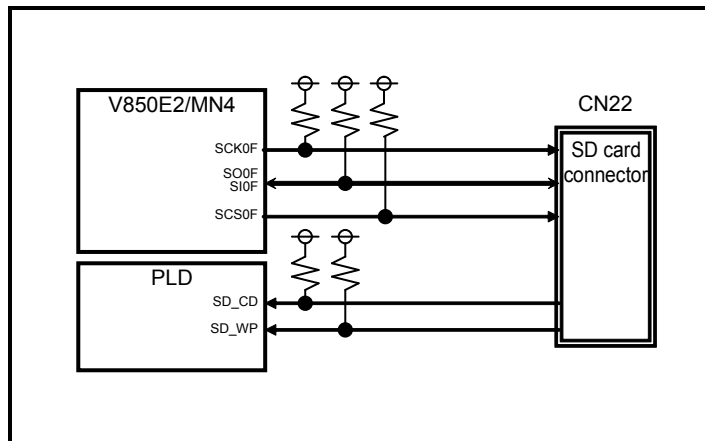
8.7. USB 2.0 Function

A USB 2.0 function device can interface with the V850E2/MN4 by using the USB function interface incorporated in the V850E2/MN4 chip.



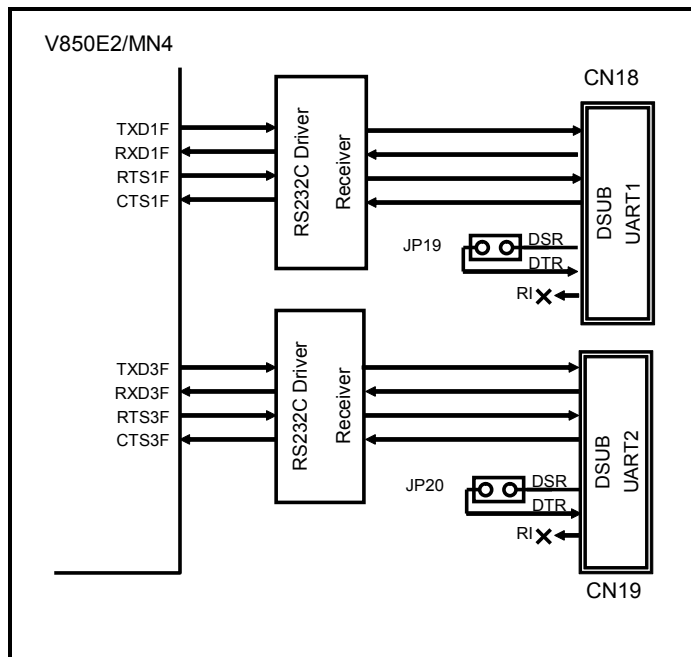
8.8. SD Interface

An SD card device can interface with the V850E2/MN4 by using the CSI interface incorporated in the V850E2/MN4 chip.



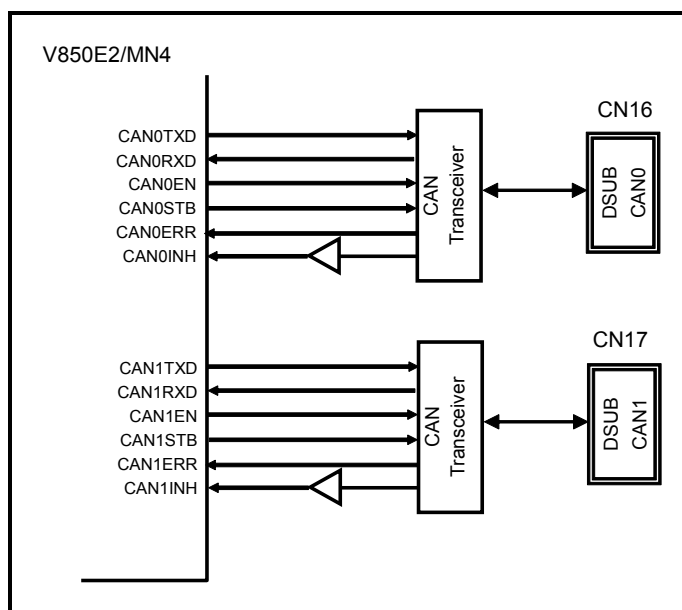
8.9. UART

A UART can interface with the V850E2/MN4 by using the UART interface incorporated in the V850E2/MN4 chip.



8.10. CAN

A CAN can interface with the V850E2/MN4 by using the CAN interface incorporated in the V850E2/MN4 chip.



8.11. LCDC

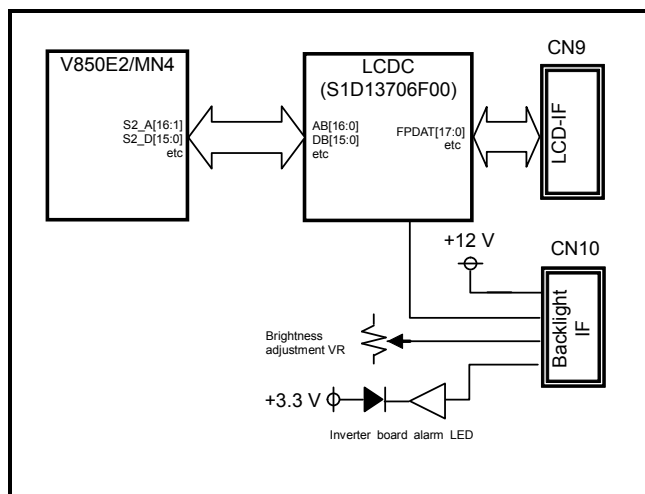
An LCD controller (the S1D13706F00 from Epson) is connected directly to the secondary bus. This controller also includes an interface for supplying power to the backlight inverter board and adjusting the brightness of the backlight.

The registers provided in the LCD controller and the internal memory addresses to which they are assigned are shown in the table below.

Address	R/W	Register Name
0xF940_0000	R	REG[00h] Revision code register
0xF940_0001	R	REG[01h] Display buffer size register
0xF940_0002	R	REG[02h] Configuration readback register
0xF940_0004	R/W	REG[04h] Memory clock configuration register
0xF940_0005	R/W	REG[05h] Pixel clock configuration register
0xF940_0008	W	REG[08h] Look-up table blue write data register
0xF940_0009	W	REG[09h] Look-up table green write data register
0xF940_000A	W	REG[0Ah] Look-up table red write data register
0xF940_000B	W	REG[0Bh] Look-up table write address register
0xF940_000C	R	REG[0Ch] Look-up table blue read data register
0xF940_000D	R	REG[0Dh] Look-up table green read data register
0xF940_000E	R	REG[0Eh] Look-up table red read data register
0xF940_000F	W	REG[0Fh] Look-up table read address register
0xF940_0010	R/W	REG[10h] Panel type register
0xF940_0011	R/W	REG[11h] MOD rate register
0xF940_0012	R/W	REG[12h] Horizontal total register
0xF940_0014	R/W	REG[14h] Horizontal display period register
0xF940_0016	R/W	REG[16h] Horizontal display period start position register 0
0xF940_0017	R/W	REG[17h] Horizontal display period start position register 1
0xF940_0018	R/W	REG[18h] Vertical total register 0
0xF940_0019	R/W	REG[19h] Vertical total register 1
0xF940_001C	R/W	REG[1Ch] Vertical display period register 0
0xF940_001D	R/W	REG[1Dh] Vertical display period register 1
0xF940_001E	R/W	REG[1Eh] Vertical display period start position register 0
0xF940_001F	R/W	REG[1Fh] Vertical display period start position register 1

0xF940_0020	R/W	REG[20h] FPLINE pulse width register
0xF940_0022	R/W	REG[22h] FPLINE pulse start position register 0
0xF940_0023	R/W	REG[23h] FPLINE pulse start position register 1
0xF940_0024	R/W	REG[24h] FPFRAME pulse width register
0xF940_0026	R/W	REG[26h] FPFRAME pulse start position register 0
0xF940_0027	R/W	REG[27h] FPFRAME pulse start position register 1
0xF940_0028	R/W	REG[28h] D-TFD GCP index register
0xF940_002C	R/W	REG[2Ch] D-TFD GCP data register
0xF940_0070	R/W	REG[70h] Display mode register
0xF940_0071	R/W	REG[71h] Special effects register
0xF940_0074	R/W	REG[74h] Main window display start address register 0
0xF940_0075	R/W	REG[75h] Main window display start address register 1
0xF940_0076	R/W	REG[76h] Main window display start address register 2
0xF940_0078	R/W	REG[78h] Main window line address offset register 0
0xF940_0079	R/W	REG[79h] Main window line address offset register 1
0xF940_007C	R/W	REG[7Ch] PIP+ window display start address register 0
0xF940_007D	R/W	REG[7Dh] PIP+ window display start address register 1
0xF940_007E	R/W	REG[7Eh] PIP+ window display start address register 2
0xF940_0080	R/W	REG[80h] PIP+ window line address offset register 0
0xF940_0081	R/W	REG[81h] PIP+ window line address offset register 1
0xF940_0084	R/W	REG[84h] PIP+ window X start position register 0
0xF940_0085	R/W	REG[85h] PIP+ window X start position register 1
0xF940_0088	R/W	REG[88h] PIP+ window Y start position register 0
0xF940_0089	R/W	REG[89h] PIP+ window Y start position register 1
0xF940_008C	R/W	REG[8Ch] PIP+ window X end position register 0
0xF940_008D	R/W	REG[8Dh] PIP+ window X end position register 1
0xF940_0090	R/W	REG[90h] PIP+ window Y end position register 0
0xF940_0091	R/W	REG[91h] PIP+ window Y end position register 1
0xF940_00A0	R/W	REG[A0h] Power save configuration register
0xF940_00A1	R/W	REG[A1h] Reserved
0xF940_00A2	R/W	REG[A2h] Reserved
0xF940_00A3	R/W	REG[A3h] Reserved
0xF940_00A4	R/W	REG[A4h] Scratch pad register 0
0xF940_00A5	R/W	REG[A5h] Scratch pad register 1
0xF940_00A8	R/W	REG[A8h] General purpose IO pins configuration register 0

0xF940_00A9	R/W	REG[A9h] General purpose IO pins configuration register 1
0xF940_00AC	R/W	REG[ACh] General purpose IO pins status/control register 0
0xF940_00AD	R/W	REG[ADh] General purpose IO pins status/control register 1
0xF940_00B0	R/W	REG[B0h] PWM clock/CV pulse control register
0xF940_00B1	R/W	REG[B1h] PWM clock/CV pulse configuration register
0xF940_00B2	R/W	REG[B2h] CV pulse burst length register
0xF940_00B3	R/W	REG[B3h] PWMOUT duty cycle register
0xF942_0000 0xF943_FFFF	R/W	80 KB display buffer



An example of setting the LCD controller is shown below. “LCDC_REG(x)” in the example indicates the register in the LCD controller for which the setting is specified (register “x”).

```

LCDC_REG(0xa8) = 0x07 ; // Specify GPIO[2:0] as outputs
LCDC_REG(0xac) = 0x00 ; // Output Low from GPIO[2:0]
                        // (GPIO[0] = DPSH, GPIO[1] = DPSV, GPIO[2]
                        // = Q/V)
LCDC_REG(0xa0) = 0x00 ; // Exit power save mode
LCDC_REG(0xad) = 0x80 ; // Output high to GPO - Backlight turns on

LCDC_REG(0x04) = 0x10 ; // BCLK:MCLK = 1:2
LCDC_REG(0x05) = 0x43 ; // PCLK = CLKI2/8 = 50 MHz/8 = 6.25 MHz
LCDC_REG(0x10) = 0x61 ; // Color LCD panel, 18 bits, TFT panel
LCDC_REG(0x12) = 49 ; // Total horizontal period = (set value +
1) * 8 = 400
LCDC_REG(0x14) = 39 ; // Horizontal display period = (set value
+ 1) * 8 = 320
LCDC_REG(0x16) = 15 ; // Horizontal display period start position
= set value + 5 = 20
LCDC_REG(0x17) = 0 ;
LCDC_REG(0x18) = 0x03 ; // Total vertical period = set value + 1 =
260
LCDC_REG(0x19) = 0x01 ;
LCDC_REG(0x1c) = 239 ; // Vertical display period = set value + 1
= 240
LCDC_REG(0x1d) = 0 ;
LCDC_REG(0x1e) = 12 ; // Vertical display period start position
= set value = 12
LCDC_REG(0x1f) = 0 ;
LCDC_REG(0x20) = 0x13 ; // Horizontal sync pulse polarity = active
low, pulse width = set value + 1 = 20
LCDC_REG(0x22) = 0x67 ; // Horizontal sync pulse start position =
set value + 1 = 360
LCDC_REG(0x23) = 0x01 ;
LCDC_REG(0x24) = 0x03 ; // Vertical sync pulse polarity = active
low, pulse width = set value + 1 = 4
LCDC_REG(0x26) = 12 ; // Vertical sync pulse start position = set
value = 12
LCDC_REG(0x70) = 0x03 ; // 8 bpp mode
LCDC_REG(0x74) = 0x00 ; // Main window display start address = 0x000
LCDC_REG(0x75) = 0x00 ;
LCDC_REG(0x76) = 0x00 ;
LCDC_REG(0x78) = 80 ; // Main window line address offset = 80
LCDC_REG(0x79) = 0 ;

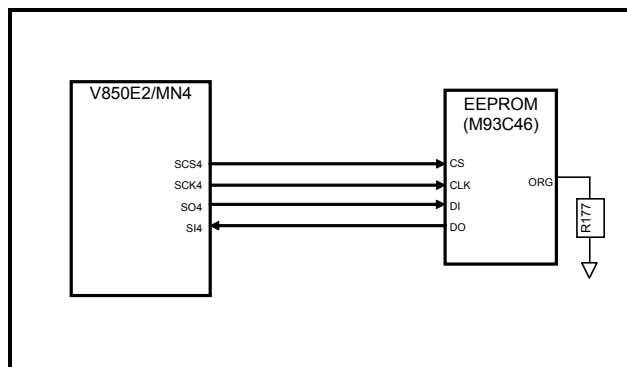
// The image is subsequently displayed on the screen after the LUT settings have been
specified.

```

8.12. EEPROM

A serial EEPROM is connected to the CSI of the V850E2/MN4.

The capacity of the serial EEPROM is 1 Kb, and the EEPROM can be accessed in a format of either 8 bits × 128 words or 16 bits × 64 words, according to whether a resistor is connected to R177 or not. The access format is 8 bits × 128 words if a 0 Ω resistor is connected to R177, and 16 bits × 64 words if no resistor is connected. The default format is 16 bits × 64 words.



8.13. Codec

The audio codec is controlled by the CPU via the I2C interface on the V850E2/MN4. Audio data is input to and output from the PLD ports using the I2S interface on the PLD.

Before using the codec, the CODEC_nRESET port on the PLD must be set to 1 (operating), and then within 10 ms, the PDN bit in the power control register on the codec must be set to 1 to specify software mode.

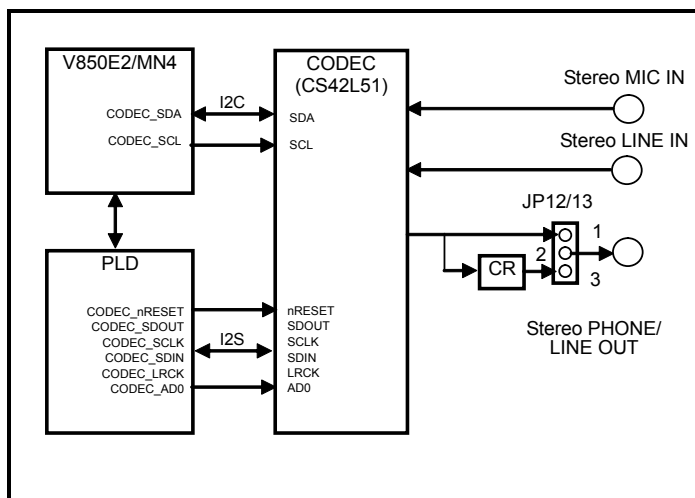
Audio data I2S, CS42L51 master mode

MCLK 12.288 MHz

Selectable sampling frequencies (Fs)

MCLKDIV2	SPEED[1:0]	Fs
0	00	96 kHz
1	01	48 kHz
1	10	24 kHz
1	11	12 kHz

Do not specify any settings other than those above.



When using DMA to transfer the audio data over the I2C interface, assign DMARQ1 for playback and DMARQ2 for recording. DMARQ1 and DMARQ2 both have negative logic. Note that the I2C interface uses the SCL2 and SDA2 pins.

An example of the procedure for playing back or recording audio data when using DMA is shown below.

1. Initialize the I2C pin settings and the I2C controller.
2. Initialize the DMA pin settings and the DMA controller.
3. Initialize the codec.
4. Start DMA.
5. Start recording or playback.

An example of setting the codec is shown below. “xxx_REG” in the example indicates the SFR in the CPU for which the setting is specified or the SFR that is referenced (register “xxx”). “I2CSend(x,y)” indicates the number of the register in the codec that was set (“x”) and the value that was set (“y”).

```
// Example of initializing DMA (No DMA transfer end interrupt is set.)
// Use Ch0 for playback
SCHCTRL0_REG = 0x00000020 ; // Do not start next DMA transaction,
                          // clear SCHSTATn.ENDn
SCHCFG0_REG = 0x00222268 ; // Specify register mode, do not start next DMA transaction,
                          // select Next0 register, specify normal mode (not write-only),
                          // specify single transfer mode, fix destination,
                          // increment source, specify transfer destination size = 32 bits,
transfer source size = 32 bits,
                          // detect DMARQ at low level, use DMARQ0
SN0DA0_REG = 0xf9000000 ;
SN0SA0_REG = DMA_PLAY_BUF_BASE ;
SN0TB0_REG = DMA_PLAY_BUF_SIZE ;

// Use Ch1 for recording
SCHCTRL1_REG = 0x00000020 ; // Do not start next DMA transaction,
                          // clear SCHSTATn.ENDn
SCHCFG1_REG = 0x00122261 ; // Specify register mode, do not start next DMA transaction,
                          // select Next0 register, specify normal mode (not write-only),
                          // specify single transfer mode, increment destination,
                          // fix source, specify transfer destination size = 32 bits,
transfer source size = 32 bits,
                          // detect DMARQ at low level, use DMARQ1
SN0SA1_REG = 0xf9000008 ;
SN0DA1_REG = DMA_REC_BUF_BASE ;
SN0TB1_REG = DMA_REC_BUF_SIZE ;
```

```

// Example of initializing codec

#define PLD_RSV_REG      (*(volatile UINT32 *) (0xf9000014))

PLD_RSV_REG = PLD_RSV_REG & 0xfffffff0 | 0x0 ; // Reset codec and set AD0 pin to 0
for(tmp_i=0 ;tmp_i<1000 ;tmp_i++){           // Wait
    PLD_RSV_REG ;
}
PLD_RSV_REG = PLD_RSV_REG & 0xfffffff0 | 0x2 ; // End codec reset and set AD0 pin to 0
for(tmp_i=0 ;tmp_i<1000 ;tmp_i++){           // Wait

I2CSend(0x02 ,0x01) ; // Address 0x02 (Power Control 1)
// 0 : Bit 7 Reserved
// 0 : Bit 6 PDN_DACB
// 0 : Bit 5 PDN_DACA
// 0 : Bit 4 PDN_PGAB
// 0 : Bit 3 PDN_PGAA
// 0 : Bit 2 PDN_ADCB
// 0 : Bit 1 PDN_ADCA
// 1 : Bit 0 PDN

I2CSend(0x03 ,0x0e) ; // Address 0x03 (MIC Power Control & Speed Control)
// 0 : Bit 7 AUTO
// 0 : Bit 6 SPEED1           96 kHz
// 0 : Bit 5 SPEED0
// 0 : Bit 4 3-ST_SP
// 1 : Bit 3 PDN_MICB
// 1 : Bit 2 PDN_MICA
// 1 : Bit 1 PDN_MICBIAS
// 0 : Bit 0 MCLKDIV2

I2CSend(0x04 ,0x4c) ; // Address 0x04 (Interface Control)
// 0 : Bit 7 SDOUT->SDIN
// 1 : Bit 6 M/S           Master
// 0 : Bit 5 DAC_DIF2           I2S, up to 24-bit data
// 0 : Bit 4 DAC_DIF1
// 1 : Bit 3 DAC_DIF0
// 1 : Bit 2 ADC_I2S/LJ           I2S
// 0 : Bit 1 DIGMIX
// 0 : Bit 0 MICMIX

I2CSend(0x05 ,0x01) ; // Address 0x05 (MIC Control)
// 0 : Bit 7 ADC_SNGVOL
// 0 : Bit 6 ADCB_DBOOST
// 0 : Bit 5 ADCA_DBOOST
// 0 : Bit 4 MICBIAS_SEL           AIN3B/MICIN2
// 0 : Bit 3 MICBIAS_LVL1           0.8xVA
// 0 : Bit 2 MICBIAS_LVL0
// 0 : Bit 1 MICB_BOOST
// 1 : Bit 0 MICA_BOOST

```

```

// Example of setting codec (using line in/out)

I2CSend(0x02 ,0x00) ; // Address 0x02 (Power Control 1)
// 0 : Bit 7 Reserved
// 0 : Bit 6 PDN_DACB
// 0 : Bit 5 PDN_DACA
// 0 : Bit 4 PDN_PGAB
// 0 : Bit 3 PDN_PGAA
// 0 : Bit 2 PDN_ADCB
// 0 : Bit 1 PDN_ADCA
// 0 : Bit 0 PDN

I2CSend(0x07 ,0x00) ; // Address 0x07 (ADCx Input Select, Invert & Mute)
// 0 : Bit 7 AINB_MUX1
// 0 : Bit 6 AINB_MUX0
// 0 : Bit 5 AINA_MUX1
// 0 : Bit 4 AINA_MUX0
// 0 : Bit 3 INV_ADCB
// 0 : Bit 2 INV_ADCA
// 0 : Bit 1 ADCB_MUTE
// 0 : Bit 0 ADCA_MUTE

```

```
#define PLD_PLAYC_REG      (*(volatile UINT32 *) (0xf9000004))
#define PLD_PLAYC_PLAY_DMAENB  (1<<2)
#define PLD_PLAYC_PLAY    (1<<3)
#define PLD_RECC_REG      (*(volatile UINT32 *) (0xf900000c))
#define PLD_RECC_REC_DMAENB  (1<<2)
#define PLD_RECC_REC      (1<<3)

// Starting playback
SCHCTRL0_REG = SCHCTRL0_REG | 0x00000001 ;           // Enable DMA
PLD_PLAYC_REG = PLD_PLAYC_PLAY_DMAENB | PLD_PLAYC_PLAY ; // Start playback

// Starting recording
SCHCTRL1_REG = SCHCTRL1_REG | 0x00000001 ;           // Enable DMA
PLD_RECC_REG = PLD_RECC_REC_DMAENB | PLD_RECC_REC ; // Start recording
```

9. CPU PIN CONNECTIONS

This section describes how each pin of the CPU in the V850E2/MN4 is used.

9.1. List of Pin Connections

Pin Name	Used As/Connected To	Refer To
P0_0 to P0_15 P1_0 to P1_15	Used as P_D0 to P_D31 primary data bus or EX_P0_0 to EX_P0_15 and EX_P1_0 to EX_P1_15	5.15
P2_0	Used as NMI	5.9
P2_1	Used as P_LLBE- or expanded EX_P2_1	5.15
P2_2	Used as P_LUBE- or expanded EX_P2_2	
P2_3	Used as P_ULBE- or expanded EX_P2_3	
P2_4	Used as P_UUBE- or expanded EX_P2_4	
P2_5	Used as P_RD- or expanded EX_P2_5	
P2_6	Used as TP1 or expanded EX_P2_6	
P2_7	Used as P_WR- or expanded EX_P2_7	
P3_0 P3_1 to P3_15	Used as expanded EX_P3_0 Used as P_A1 to P_A15 or expanded EX_P3_1 to EX_P3_15	5.15
P4_0 to P4_5 P4_6 P4_7 P4_8 P4_9 P4_10 P4_11 P4_12 P4_13	Used as P_A16 to P_A21 or expanded EX_P4_0 to EX_P4_5 Used as RXD3F or expanded EX_P4_6 Used as TXD3F or expanded EX_P4_7 Used as P_CS1- or expanded EX_P4_8 Used as P_CS2- or UVBUSF- Used as expanded EX_P4_9 Used as P_CS3- or UVBUSDETF Used as expanded EX_P4_10 Used as SCK0F or expanded EX_P4_11 Used as SO0F or expanded EX_P4_12 Used as SI0F or expanded EX_P4_13	5.15 8.8
P5_0 P5_1 P5_2 P5_3 P5_4 P5_5 P5_6 P5_7	Connected to CRS/PHYAD4 on LAN8700iC Connected to COL/RMII/CRS_DV on LAN8700iC Connected to TXD3 on LAN8700iC Connected to TXD2 on LAN8700iC Connected to TXD1 on LAN8700iC Connected to TXD0 on LAN8700iC Connected to TX_EN on LAN8700iC Connected to TX_CLK on LAN8700iC	8.5

P5_8	Connected to nINT/TX_ER/TXD4 on LAN8700iC	
P5_9	Connected to RX_ER/RXD4 on LAN8700iC	
P5_10	Connected to RX_CLK/REGOFF on LAN8700iC	
P5_11	Connected to RX_DV on LAN8700iC	
P5_12	Connected to RXD0/MODE0 on LAN8700iC	
P5_13	Connected to RXD1/MODE1 on LAN8700iC	
P5_14	Connected to RXD2/MODE2 on LAN8700iC	
P5_15	Connected to RXD3/nINTSEL on LAN8700iC	
P6_0	Connected to MDC on LAN8700iC	
P6_1	Connected to MDIO on LAN8700iC	
P7_0 to P7_15	Used as S1_D0 to S1_D31 and S2_D0 to S2_D31 secondary	5.16
P8_0 to P8_15	data bus or TP7_0 to TP7_15 and TP8_0 to TP8_15	
P9_0	Used as S_SDCKE	
P9_1	Used as S_BUSCLK1/2	
P9_2	Used as S_SDCAS-	
P9_3	Used as S_SDRAS-	
P9_4	Used as S_LLDQM	
P9_5	Used as S_LUDQM	
P9_6	Used as S_ULDQM	
P9_7	Used as S_UUDQM	
P9_8	Used as SCS4	8.12
P9_9	Used as SO4	
P9_10	Used as SI4	
P9_11	Used as SCK4	
P9_12	Used as S_RD-	
P9_13	Used as S_WR-	
P9_14	Used as S_LLBE-	
P9_15	Used as S_LUBE-	
P10_0	Used as S_ULBE-	
P10_1	Used as S_UUBE-	
P10_2	Used as S_WE-	
P10_3	---	
P10_4	Used as S_CS0-	7.1
P10_5	Used as S_CS1-	8.2
P10_6	Used as S_CS2-	8.11
P10_7	Used as S_SDCS-	7.2

P10_8	Used as WAIT-	
P10_9	Used as PAD1	
P10_10	Used as PAD2	
P10_11	Used as SCS0F-	
P11_0 to P11_13	Used as S1_A1 to S1_A14 or S2_A1 to S2_A14 secondary address bus	
P11_14 to P11_15	Used as S2_A15 to S2_A16 secondary address bus	
P12_0 to P12_4	Used as S2_A17 to S2_A21 secondary address bus	
P12_5	Used as INTP5	
P12_6	Used as HA23	
P12_7	Used as HA24	
P12_8	Used as HA25 or CODEC_SDA	
P12_9	Used as CODEC_SCL	8.13
P13_0	Used as UCLK or S_DMARQ0	
P13_1	Used as S_DMAAK0	
P13_2	Used as UPONH or S_DMARQ1	
P13_3	Used as UOCIH or SDMAAK1	
P13_4	Used as CAN0TXD and TXD1F	8.10
P13_5	Used as CAN0RXD or RXD1F (TP2)	
P13_6	Used as CAN1TXD	
P13_7	Used as CAN1RXD (TP3)	
P14_0	---	
P14_1	---	
P14_2	Used as CAN0ERR-	8.10
P14_3	Used as CAN1ERR-	
P14_4	Used as CAN0INH-	
P14_5	Used as CAN1INH-	