

## RTE-V852/3-PC SUPPLEMENTARY MANUAL NO.2 (REV.1.0)

### 1. BREAKPOINT

#### 1.1. IMPLEMENTATION OF A BREAKPOINT

The common CPU has an instruction having the same length as the shortest instruction that can be used for a breakpoint. This type of instruction is often called a breakpoint instruction or trap instruction. Unfortunately, the V850 CPU has no instruction that can be used for a breakpoint. The V850 CPU has a trap instruction of four bytes long, which is longer than the shortest instruction of two bytes long.

If an instruction longer than the shortest instruction is used for a breakpoint, a failure may occur. This manual does not detail possible failures. An example of the possible failures is this: There is a two-byte instruction at the location at which a breakpoint is set; A jump may be made to the instruction at the next location.

The RTE-V852/3-PC implements a safe breakpoint as described below:

- 1) Uses a branch-myself instruction (branch instruction to an address of  $\pm 0$  relative to 0x8505 in binary) as a breakpoint instruction.
- 2) Assumes that a break occurs when the following conditions are all satisfied: An interval timer interrupt used by the Multi ROM monitor occurs, and the instruction at the return address is 0x8505; and the address is included in the breakpoint list.

The interval timer interrupt is used to determine the profiler period. The interrupt interval can be set by SW1 on the base board. The default interval is 60 Hz.

#### 1.2. RESTRICTIONS

Because of the breakpoint method described above, the following restrictions are imposed:

- 1) The interval timer interrupt cannot be stopped (inhibited).
- 2) It takes a while for a break to occur after the corresponding breakpoint in the program is executed. The maximum length of this delay equals the interrupt period of the interval timer. This delay generally causes no problems. In an application using a maskable interrupt, however, the delay may cause the problem of 3) below.
- 3) If a maskable interrupt that can be accepted occurs during a period from when a breakpoint of a program is executed until the corresponding break occurs, the interrupt will be accepted. If the interrupt handler also contains a breakpoint, a break occurs at the breakpoint. In addition, an interrupt with higher priority may be accepted while the actual break is being waited for at that breakpoint.