RTE-V*R*4300-PC

User's Manual

Midas lab

REVISION HISTORY

Date	Rev	Explanation of revision
October 15, 1996	1.0	First edition (The previously-edited manual has been modified according to the change of the circuit board that corresponds to the 133-MHz RTE-VR4300-PC.)
January 9,1998	1.1	Changed the figure of JP4 at 3.10ROMSEL JUMPER (JP4)....page10 Changed the figure of External Interrupts at 5.5INTERRUPT.......page27

CONTENTS

1. INTRODUCTION

This manual describes the **RTE-VR4300-PC**, which is an evaluation board for the VR4300, NEC's CPU. With the RTE-VR4300-PC, it is possible to develop and debug programs, and evaluate the CPU performance, using the GreenHills Multi debugger. Communication with this debugger is carried out using the IBM-PC/AT ISA bus or RS-232C serial interface. It is also possible to expand memory and I/O units using local bus connectors provided on the evaluation board.

1.1. NUMERIC NOTATION

This manual represents numbers according to the notation described in the following table. Hexadecimal and binary numbers are hyphenated at every four digits, if they are difficult to read because of many digits being in each number. Letter x is used to represent an arbitrary numeral in a number, like "1FxxH."

Number	Notation rule	Example
Decimal number	Only numerals are indicated.	"10" represents number 10 in decimal.
Hexa-decimal number	A number is suffixed with letter H.	"10H" represents number 16 in decimal.
Binary number	A number is suffixed with letter B.	"10B" represents number 2 in decimal.

Number Notation Rules

2. FEATURES AND FUNCTIONS

The overview of each function block of the RTE-VR4300-PC is shown below.
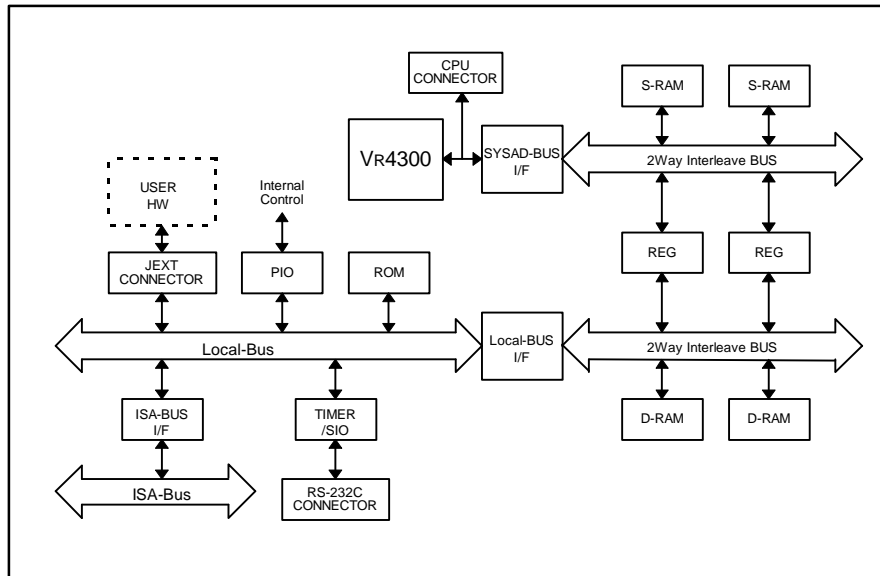
RTE-VR4300-PC Block Diagram

Features

- ROM: 256 Kbytes (64K x 16 bits x 2)
- SRAM: 512 Kbytes (64K x 16 bits x 4)
- DRAM: 8, 16, or 32 Mbytes (standard of 8 Mbytes) installed in 72-pin SIMM sockets
- RS-232C port (9-pin D-SUB connector)
- Communication function supported using the ISA bus of a PC/AT or compatible
- Local bus connector for user-installed expansion equipment
- Processor pin connector enabling measurement of all CPU signals
- External reset switch provided on the rear panel
- Connection pins for ROM in-circuit debugger

3. BOARD CONFIGURATION

The physical layout of the major components on the RTE-VR4300-PC board is shown below. This chapter explains each component.
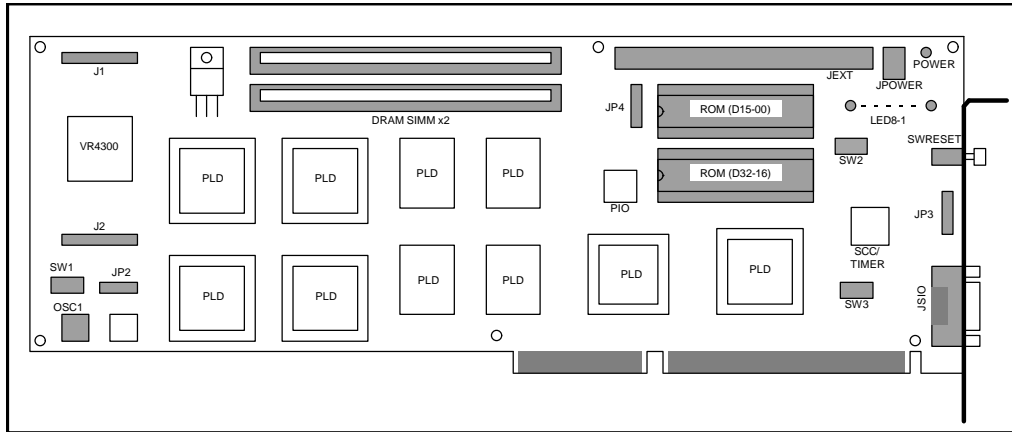
RTE-VR4300-PC Board Top View

3.1. RESET SWITCH (SWRESET)

SWRESET is a reset switch.   Pressing this switch causes the CPU to be reset.

3.2. POWER SUPPLY CONNECTOR (JPOWER)

When this board is to be used as a standalone, that is, without being inserted in an ISA bus slot, the board should be supplied with power from an external power supply by connecting it to the JPOWER connector.

The external power should be one rated as listed below.

> Voltage: 5 V
>
> Current: Maximum of 3.0 A (excluding the current supplied to the JEXT connector)
>
> Mating connector: Type A (5.5 mm in diameter)
>
> Polarity:
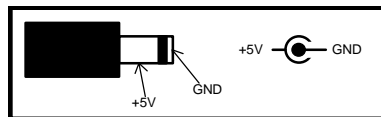
[Caution]   When attaching an external power supply to the board, be <u>careful about its connector polarity</u>.   When inserting the board into the ISA bus slot, do not attach the JPOWER connector to an external power supply.

3.3. CLOCK SOCKET (OSC1)

OSC1 is an 8-pin socket for an oscillator to generate clock pulses supplied to the CPU.   The socket is factory-equipped with a 66.6-MHz oscillator.   When exchanging it, be careful about its polarity.

[Caution]   When you have to cut an oscillator pin for convenience, be careful not to cut it too short, or otherwise the frame (housing) of the oscillator may touch a tine in the socket, resulting in a short-circuit occurring.

3.4. CPU SWITCH (SW1)

SW1 is a switch for determining the operation mode of the VR4300.   It is set as listed below.

SW1 contact	Function
1	ON: Little endian OFF: Big endian (default)
2	Not used (fixed at OFF)
3	ON: DIVMODE0 = 0 (Low) OFF: DIVMODE1 = 1 (High)
4	ON: DIVMODE1 = 0 (Low) OFF: DIVMODE1 = 1 (High)
5	Not used (fixed at OFF)
6	Not used (fixed at OFF)
7	Not used (fixed at OFF)
8	ON: 64-bit monitor OFF: 32-bit monitor (default)

SW1 Setting

[Caution]   The VR4300 endians are <u>set by software</u> in the CPU internal registers.   This switch is used by an external circuit to determine the byte position and ROM bank.

[Memo]   SW1-8 is used to select the monitor stored in the selected ROM address bank.

3.5. CONFIG SWITCH (SW2)

SW2 is a switch for general-purpose input ports.   When a switch contact is open, it corresponds to 1.   When it is closed, it corresponds to 0.   See Section 5.2.2 for details.

3.6. ISA-PORT SWITCH (SW3)

SW3 is a switch for selecting the I/O address of the ISA bus.   Switch contacts 1 to 8 corresponds to ISA addresses A4 to A11, respectively (A12 to A15 are fixed at 0).   This means that the I/O address that can be selected ranges between 000xH and 0FFxH.   When a switch contact is open, it corresponds to 1.   When it is closed, it corresponds to 0.

SW3 contact	1	2	3	4	5	6	7	8
ISA address	A4	A5	A6	A7	A8	A9	A10	A11

SW3-to-ISA Address Correspondence

3.7. LED-POWER AND LED8 TO LED1

LED-POWER lights when power is supplied.   LED8 to LED1 can be turned on and off from general-purpose output ports.   See Section 5.2.3 for details.

3.8. SYNC JUMPER (JP2)

JP2 can set the delay time of the SYNC-OUT/SYNC-IN in the CPU between 0 ns and 5 ns in 1-ns units.   Usually, it should be set to 1 ns.

JP2 jumper setting	1-2	3-4	5-6	7-8	9-10	11-12
SYNC delay time	0ns	1ns (default)	2ns	3ns	4ns	5ns

JP2 Setting

3.9. ROMEMU JUMPER (JP3)

JP3 is a set of jumper pins which are set to use mainly the ROM in-circuit debugger.   It enables a reset and an interrupt from the ROM in-circuit debugger.

JP3 pin	Function	JP3 pin	Function
1	RESET input (active-low) 47 kΩ pull-up resistor	2	INT0 input (active-low) 47 kΩ pull-up resistor
3	NMI input (active-low) 47 kΩ pull-up resistor	4	INT1 input (active-low) 47 kΩ pull-up resistor
5	Not used(NC)	6	INT2 input (active-low) 47 kΩ pull-up resistor
7	Not used(NC)	8	INT3 input (active-low) 47 kΩ pull-up resistor
9	Not used(NC)	10	INT4 input (active-low) 47 kΩ pull-up resistor
11	**GND**	12	**GND**

JP3 Functions

3.10. ROMSEL JUMPER (JP4)

JP4 is a set of jumper pins for specifying the type of ROM to be installed in the ROM socket. Its pins correspond to ROM addresses as shown below. The ROM has four banks that can be selected by switching the upper address bits so that the system endians are supported.
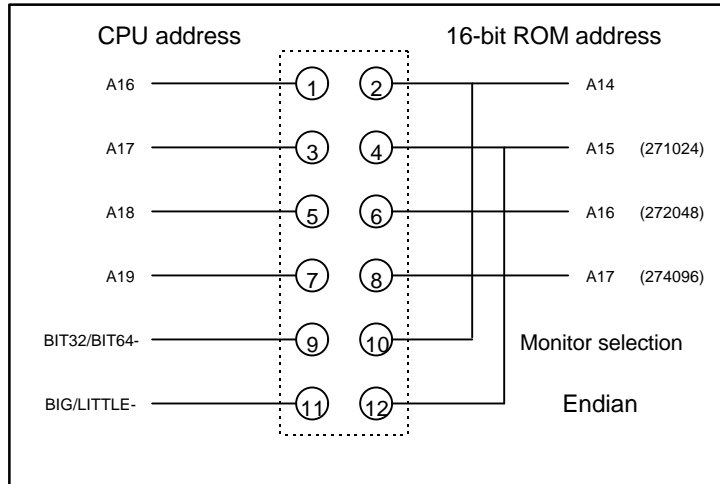
JP4 Connection

The table below lists the relationships between the ROM types and jumper pins to be strapped.

ROM type	Pin connection (with a bank)	Pin connection (with no bank)
271024 (64Kx16Bit)	9-10, 11-12 (factory-set)	1-2, 3-4
272048 (128Kx16Bit)	-	1-2, 3-4, 5-6
274096 (256Kx16Bit)	-	1-2, 3-4, 5-6, 7-8

JP4 Pin Connection

3.11. SERIAL CONNECTOR (JSIO)

JSIO is a connector for the RS-232C interface controlled by the serial controller (SCC2691). It is a 9-pin D-SUB connector (D-SUB9) generally used with the PC/AT. All signals at this connector are at RS-232C level. Its pin arrangement and signal assignment are shown and listed below.

For connection signals connected to the host computer, the table gives the wirings for both the D-SUB9 pins and D-SUB25 pins on the host side. (These are general cross-cable wirings.)
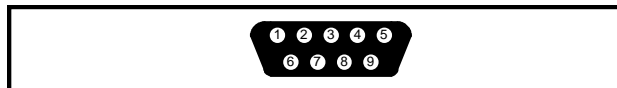
JSIO Pin Arrangement

JSIO pin	Signal name	Input/ output	Connector pin number on the host side	
			D-SUB9	D-SUB25
1	NC			
2	RxD(RD)	Input	3	2
3	TxD(SD)	Output	2	3
4	DTR(DR)	Output	1, 6	6, 8
5	GND		5	7
6	DSR(ER)	Input	4	20
7	RTS(RS)	Output	8	5
8	CTS(CS)	Input	7	4
9	NC			

JSIO Connector Signals

3.12. JEXT CONNECTOR

JEXT is a connector mating with the EXT-BUS connector for a user-installed expansion unit. See Section 5.6 for details of the EXT-BUS.

3.13. CPU TEST PINS (J1 AND J2)

J1 and J2 are connectors for CPU signals.   They are used to extend signals lines for testing or circuit expansion purposes.

> **[Memo]**   The mating connector for the J1 and J2 is: FX4B1-40S-1.27SV (HIROSE), which is a 1.27 mm pitch, surface-mount connector

J1 pin	Signal name	J1 pin	Signal name
1	SYSAD[0]	2	SYSAD[1]
3	SYSAD[2]	4	SYSAD[3]
5	SYSAD[4]	6	SYSAD[5]
7	SYSAD[6]	8	SYSAD[7]
9	**GND**	10	-
11	SYSAD[8]	12	SYSAD[9]
13	SYSAD[10]	14	SYSAD[11]
15	SYSAD[12]	16	SYSAD[13]
17	SYSAD[14]	18	SYSAD[15]
19	**GND**	20	-
21	SYSAD[16]	22	SYSAD[17]
23	SYSAD[18]	24	SYSAD[19]
25	SYSAD[20]	26	SYSAD[21]
27	SYSAD[22]	28	SYSAD[23]
29	**GND**	30	-
31	SYSAD[24]	32	SYSAD[25]
33	SYSAD[26]	34	SYSAD[27]
35	SYSAD[28]	36	SYSAD[29]
37	SYSAD[30]	38	SYSAD[31]
39	**+3.3V**	40	-

J1 Pin Arrangement

J2 pin	Signal name	J2 pin	Signal name
1	SYSCMD[0]	2	SYSCMD[1]
3	SYSCMD[2]	4	SYSCMD[3]
5	SYSCMD[4]	6	-
7	**GND**	8	**GND**
9	PMASTER-	10	EOK-
11	PVALID-	12	EVALID-
13	PREQ-	14	EREQ-
15	-	16	MasterCLOCK
17	**GND**	18	**GND**
19	INT[0]-	20	INT[1]-
21	INT[2]-	22	INT[3]-
23	INT[4]-	24	NMI-
25	RESET-	26	ColdRESET-
27	**+3.3V**	28	**+3.3V**
29	(SW1-1)	30	DIVMODE[0] (SW1-3)
31	(SW1-2)	32	DIVMODE[1] (SW1-4)
33	**GND**	34	**+5V**
35	-	36	**GND**
37	**GND**	38	TCLOCK
39	**+3.3V**	40	**+3.3V**

J2 Pin Arrangement

3.14. DRAM-SIMM SOCKETS

The RTE-VR4300-PC has two DRAM-SIMM sockets used to install 4 Mbytes (standard) of SIMM. Each socket can hold a 72-pin 4-, 8-, or 16-Mbyte SIMM (known as a module for DOS/V machines), so it is easy to expand the capacity of DRAM.

The capacity of installed SIMMs can be detected using a PIO port.   (See Section 5.2.2.)

3.15. ROM SOCKETS

The RTE-VR4300-PC has ROM sockets. Of these sockets, two are used to hold 40-pin ROM chips to provide standard 128 Kbytes (64K x16 bits).   The access time of the ROM chips used here should be 150 ns or less.   The ROM has four banks that can be selected using switches to allow for selection of endian and operation mode. See Section 3.10 for bank setting.

4. INSTALLATION AND USE

The RTE-VR4300-PC board is designed to be installed in the ISA bus slot of a PC/AT or compatible (hereafter called the PC).   However, it can also be used as a standalone, if it is powered from an external power supply.   When the board is used for testing purposes or with the Multi debugger, communication software called RTE for Windows must be installed in the PC.   Refer to the **RTE for Windows Installation Manual** for installation and test methods.

4.1.   BOARD SETTING

The RTE-VR4300-PC board has DIP switches.   The DIP switches can be used to set up the evaluation board.   The switch layout is shown below.
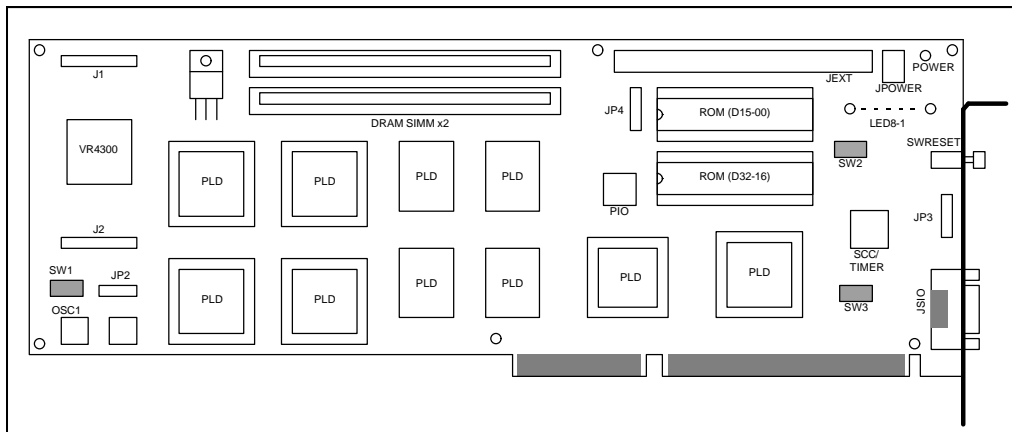
Switches on the RTE-VR4300-PC Board

SW1 is used to set the CPU operation mode, endian, and internal clock.

SW1 contact	Function
1	ON: Little endian OFF: Big endian (default)
2	Not used (fixed at OFF)
3	ON: DIVMODE0 = 0 (Low)) OFF: DIVMODE0 = 1 (High)
4	ON: DIVMODE1 = 0 (Low) OFF: DIVMODE1 = 1 (High)
5	ON: DIVMODE2 = 0 (Low) OFF: DIVMODE2 = 1 (High)
6	Not used (fixed at OFF)
7	Not used (fixed at OFF)
8	ON: 64-bit monitor OFF: 32-bit monitor (default)

SW1 Setting

SW2 is a switch for general-purpose input ports. For the Multi monitor in the factory-installed ROM, SW2 is used to set the RS-232C baud rate, profiler timer period, and VR4300 data rate.

SW2 contact	1	2	Baud rate
Setting	ON	ON	Not used
	OFF	ON	38400 baud
	ON	OFF	19200 baud
	OFF	OFF	9600 baud (factory-set)

Baud Rate Setting

SW2 contact	3	4	Profiler period
Setting	ON	ON	Timer interrupt is not used.
	OFF	ON	200 Hz 5ms
	ON	OFF	100 Hz 10ms
	OFF	OFF	60 Hz 16.67ms (factory-set)

Profiler Period Setting

SW2 contact	5	6	Data rate
Setting	x	ON	Dxx
	x	OFF	D (factory-set)

Data Rate Setting

Contacts 7 and 8 of SW2 are not used for the Multi monitor (they are fixed at OFF).

SW3 is a switch for selecting the I/O address of the ISA bus. Switch contacts 1 to 8 correspond to ISA addresses A4 to A11, respectively (A12 to A15 are fixed at 0). This means that the I/O address that can be selected ranges between 000xH and 0FFxH. When a switch contact is open, it corresponds to 1. When it is closed, it corresponds to 0. Generally, SW3 is set to any value between 20xH and 3FxH.

SW3 contact	1	2	3	4	5	6	7	8	
Address	A4	A5	A6	A7	A8	A9	A10	A11	I/O address
ON/ OFF	0	0	0	0	0	1	0	0	020xH (factory-set)

SW3-to-ISA I/O Address Correspondence

[Caution] Allocate the I/O address of the ISA bus to an address not in use, referring to the manual of the used PC or other installed adapter boards.

4.2.   INSTALLATION ON THE ISA BUS

When the RTE-VR4300-PC is installed in the ISA bus slot of the PC, power (+5V) is supplied from the ISA bus to the board.   In addition, the ISA bus can be used for communication with the debugger, so programs are down-loaded at high speed.

The RTE-VR4300-PC can be installed in the ISA bus slot according to the following procedure.

<1> Set the I/O address of the PC using a DIP switch on the board.   Be careful not to specify the same I/O address as used for any other I/O unit.   See Section 4.1 for switch setting.

<2> Turn off the power to the PC, open its housing, and confirm the ISA bus slot to be used.   If the slot is equipped with a rear panel, remove the rear panel.

<3> Insert the board into the ISA bus slot.   Make sure that the board does not touch any adjacent board.   Fasten the rear panel of the board to the housing of the PC with screws.

<4> Turn on the power to the PC, and check that the POWER-LED on the board lights.   **If the LED does not light, turn off the PC power immediately, and check the connection**.   If the system does not start normally (for example, if an error occurs during installation of a device driver), it is likely that the set I/O address is the same as one already in use. Reconfirm the I/O address of the board by referring to the applicable manual of the PC or the board.

<5> When the system turns out to be normal, turn off the PC power again, and put back its housing.

4.3.   STANDALONE USE OF THE BOARD

When the RTE-VR4300-PC is used as a standalone rather than being installed in the PC, it requires an external power supply.   In addition, communication with the debugger is supported only by the RS-232C interface.   This configuration is useful when the host debugger used with the board is not one in the PC/AT or compatible as well as when the board is used for hardware confirmation and expansion.

The RTE-VR4300-PC can be used as a standalone according to the following procedure.

<1> Get an RS-232C cable for connection with the host and an external power supply (+5 V, 3 A) on hand.   Especially for the power supply, **watch for its voltage and connector polarity**.   In addition, attach spacers to the four corners of the board, so it will not pose any problem wherever it is installed.   See Sections 3.11 and 3.2 for RS-232C cable connection and the power supply connector, respectively.

<2> Set the RS-232C baud rate using a DIP switch on the board.   See Section 4.1 for switch setting.

<3> Connect the board to the host via an RS-232C cable.   Also connect an external power supply to the JPOWER connector, then check that the POWER-LED on the board lights. **If the LED does not light, turn off the power immediately, and check the connection**.

5. HARDWARE REFERENCES

This chapter describes the hardware of the RTE-VR4300-PC.

5.1. MEMORY MAP

The memory assignment of the board is shown below.
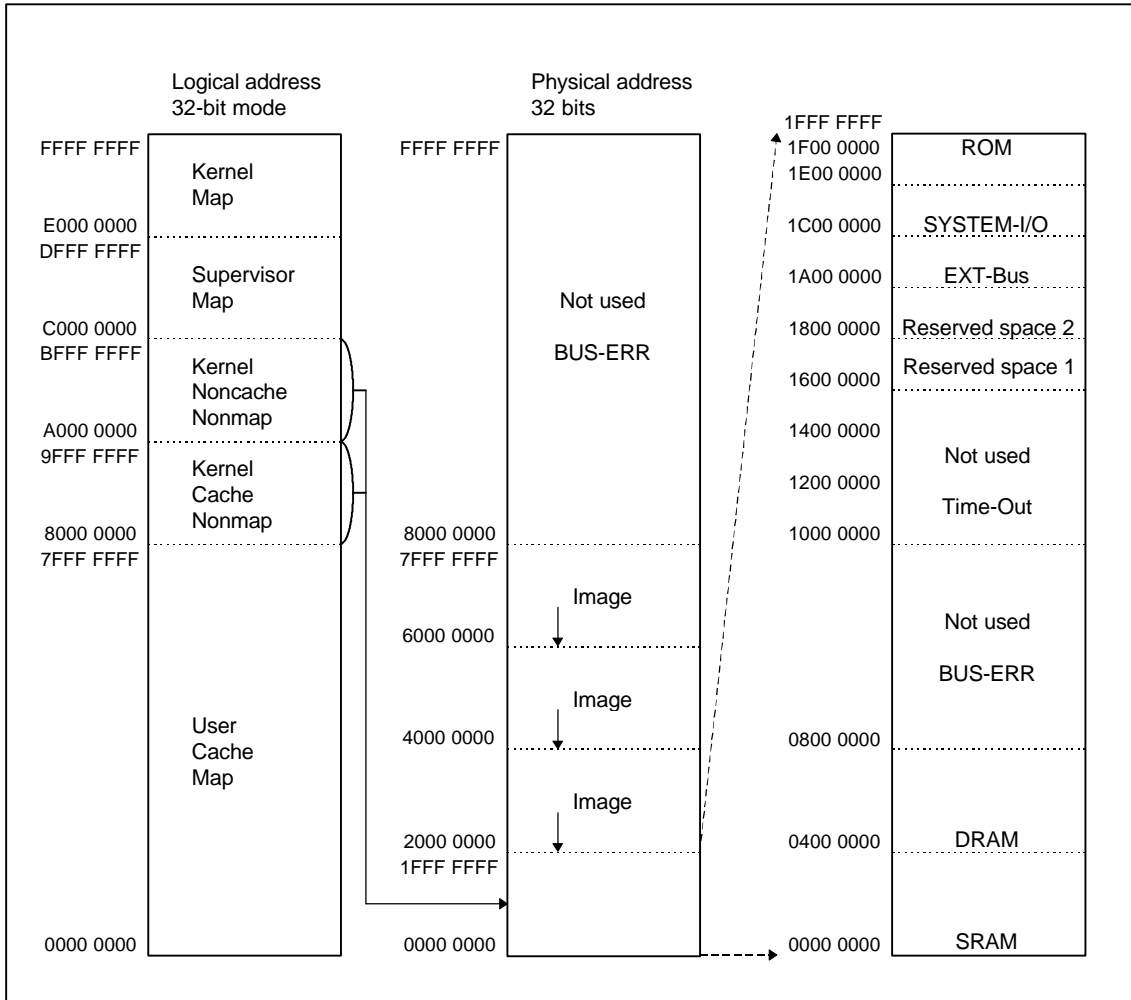
Memory Map

The VR4300 has a memory management feature.   It converts logical addresses to physical addresses.   When the Multi monitor is used, programs are executed in the kernel space (8000-0000H to BFFF-FFFFH) where a TLB map is not used.   When a cache is used, 8000-0000H is added to physical addresses to determine logical addresses.   When a cache is not used, A000-0000H is added.

BUS-ERR (0800-0000H to 0FFF-FFFFH, 8000-0000H to FFFF-FFFFH), not used

If this space is accessed, a bus error occurs.

TIME-OUT (1000-0000H to 15FF-FFFFH), not used

If this space is accessed, a time-out (about 8 μs) interrupt occurs.

Reserved space 1 (1600-0000H to 17FF-FFFFH)

Reserved space 2 (1800-0000H to 19FF-FFFFH)

These spaces are reserved for future use.   Do not try to access them.

SRAM space (0000-0000H to 0007-FFFFH)

This space is provided in SRAM on the board.   Its capacity is 512 Kbytes.   SRAM can be accessed with no wait state, as either a cache or noncache space.

DRAM space (0400-0000H to 07FF-FFFFH)

This space is provided in the 72-pin SIMMs on the board.   Two 4M-byte SIMM chips are already installed.   So the total capacity is 8 Mbytes.   Memory can be expanded by replacing the 4-Mbyte SIMM chips with 8- or 16-Mbyte SIMM chips.   This space can be accessed as either a cache or noncache space.

EXT-BUS (1A00-0000H to 1AFF-FFFFH)

This space is used for a hardware expansion board connected to the JEXT connector on the RTE-VR4300-PC.   See Section 5.6 for details of the EXT-BUS.   It can be accessed only as a noncache space in halfword (16-bit) units.

SYSTEM-I/O (1C00-0000H to 1CFF-FFFFH)

This space is assigned to I/O devices for controlling each function on the board.   It acts as memory-mapped I/O units.   See Section 5.2 for details.   It can be accessed as a noncache space.

ROM (1F00-0000H to 1FFF-FFFFH)

This space is provided in ROM on the board. Its storage capacity is 256 Kbytes. Its access time is 150 ns or less.   It can be accessed as either a cache or noncache space.

The standard ROM chip that is factory-set contains the Multi monitor.

5.2.   SYSTEM-I/O

SYSTEM-I/O is an I/O device mapped in a memory space.   The I/O devices include the UART/TIMER, PIO, and ISA bus interface.

The SYSTEM-I/O is designed to be accessed as a kernel noncache space.   So, the following explanation uses logical addresses.   In addition, data bus D[7..0] is connected, and it is necessary to take endians into account during byte access.   When byte access is carried out with a big endian, 3 is added as a byte offset.

Logical address	I/O device
BC00-00xxH	UART/TIMER (SCC2691)
BC00-01xxH	PIO (μPD71055)
BC00-02xxH	LED/SWITCH
BC00-03xxH	ISA-BUS I/F

SYSTEM-I/O Device Map

Basically, the board is used on a dedicated monitor program.   So, the explanation of the ISA bus interface is left out.   (The user program is prohibited from accessing the ISA bus interface.)

5.2.1. UART/TIMER (SCC2691)

The SCC2691 UART receiver/transmitter LSI chip produced by PHILIPS Signetics is used as the UART/TIMER.   Because the SCC2691 has a 3-character buffer in the receiver section, it is possible to minimize chances of an overrun error occurring during reception.   Moreover, a 3.6864 MHz oscillator is connected across the X1 and X2 pins.   It, in conjunction with a 16-bit counter in the SCC2691, enables measurement of about 271 ns to 17.8 ms.

Each register in the SCC2691 is assigned as listed below.   Refer to the applicable SCC2691 manual for the function of each register.

Logical address	Read access	Write access
BC00-0000H	MR1,MR2	MR1,MR2
BC00-0008H	SR	CSR
BC00-0010H	Reserved	CR
BC00-0018H	RHR	THR
BC00-0020H	Reserved	ACR
BC00-0028H	ISR	IMR
BC00-0030H	CTU	CTUR
BC00-0038H	(CTL)	CTLR

SCC2691 Register Map

The general-purpose output pin (MPO) and input pin (MPI) are used as RTS (RS) and CTS (CS), respectively.   DTR (DR) and DSR (ER) are controlled by the PIO.   See Section 5.2.2 for details.

5.2.2. PIO (μPD71055)

The μPD71055 produced by NEC is installed as a PIO.   The μPD71055 is compatible with the i8255 produced by Intel.   It has three parallel ports.   These ports are used for various types of control.   Each register of the PIO is assigned as listed below.

Logical address	Read access	Write access
BC00-0100H	PORT0	PORT0
BC00-0108H	PORT1	PORT1
BC00-0110H	PORT2	PORT2
BC00-0118H	---------	CMD REG

PIO Register Map

At a reset, all PIO ports are set as input, so the signal state of bits used for output is set to a high level, using a pull-up resistor.   The following table lists the way each port bit is used.

Port	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PORT0				Out				
PORT0			**Lwid[1]**	**Lwid[0]**	1 (fixed)	1 (fixed)	1 (fixed)	1 (fixed)
PORT1				Out				
PORT1	-	-	**Swait[1]**	**Swait[0]**	**NOILV**	**NOHIT**	**Dwid[1]**	**Dwid[0]**
PORT2		In				Out		
PORT2	**PD2**	**PD1**	**TOVF-**	**DSR-**	**DTR-**	**IRQ MASK**	**TOVF CLR-**	1 (fixed)
CMD (Init)	1	0	0	0	1	0	0	0

PIO Bit Map

The following paragraphs explain the meaning of each port bit.

Lwid[1..0]: The minimum number of cycles is specified for local bus access. The number of cycles is based on the LBCLK pulse generated by dividing the frequency of the TCLOCK by 2. See Section 5.3.3 for detailed timing descriptions.

Lwid[1]	Lwid[0]	Number of cycles
0	0	4
0	1	1
1	0	2
1	1	3

Lwid[1..0] Setting

Swait[1..0]: The number of wait states is specified for the SRAM read cycle. See Section 5.3.1 for detailed timing descriptions.

Swait[1]	Swait[0]	Number of wait states
0	0	0
0	1	1
1	0	2
1	1	3

Swait[1..0] Setting

Dwid[1..0]: The RAS/CAS width is specified for the DRAM access cycle. See Section 5.3.2 for detailed timing descriptions.

Dwid[1]	Dwid[0]	RAS precharge	RAS (Min) active	CAS (Read) active	CAS (Write) active
0	0	2	3	1	1
0	1	3	4	2	1
1	0	4	5	3	2
1	1	5	6	4	3

Dwid[1..0] Setting

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NOILV:　This bit specifies whether to select the interleave mode for DRAM access.　When 0, it selects the interleave mode.　When 1, it deselects the interleave mode.

NOHIT:　This bit specifies whether to enable a page hit for DRAM access.　When 0, it enables a page hit.　When 1, it disables a page hit.

TOVF-:　This bit becomes 0 when the local bus cycle is 8 μs or longer and a time-out occurs. The flag is cleared (1), using bit 1 (TOVFCLR-) of port 2.

TOVFCLR-:　This bit clears (1) bit 5 of port 2.　It should be initialized to 1 and usually kept to be 1.　When TOVF- is to be cleared, the bit should be reset to 0, then set back to 1.

IRQMASK:　This bit controls the mask of interrupts (INT0 to INT2) to the CPU.　When set to 1, it masks interrupts, using a gate.　It is initialized to 1.　After interrupts become acceptable, it should be reset to 0.

DTR-:　This bit controls the DTR signal output from the JSIO connector.　The inverted state of this bit is converted to the RS-232C level and output to the JSIO connector.

DSR-:　This bit indicates the state of the DSR signal input from the JSIO connector.　The state of this bit represents the inverted state of the DSR signal at the JSIO connector.

PD[2..1]:　PD[2..1] of the DRAM (72-pin SIMM) on the board can be accessed.　The states of these bits indicate the size of the DRAM area on the board.　The table below lists the relationships between PD[2..1] and the DRAM capacity.

PD[2]	PD[1]	DRAM capacity
0	0	4 Mbytes
0	1	Reserved
1	0	16 Mbytes
1	1	8 Mbytes

PD[2..1] and DRAM Capacity

5.2.3.　SWITCH/LED (General-Purpose Input/Output) Ports

The SWITCH/LED port is an 8-bit input/output port provided on the board.　It is used to read the state of the SW2-CONFIG DIP switch and turn on the LEDs (LED[8..1]).

| Logical address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Function
BC00-0200H input	SW2-8	SW2-7	SW2-6	SW2-5	SW2-4	SW2-3	SW2-2	SW2-1	0 = ON 1 = OFF
BC00-0200H output	LED-8	LED-7	LED-6	LED-5	LED-4	LED-3	LED-2	LED-1	0 = ON 1 = OFF

SWITCH/LED Port Bit Map

5.3.   BUS CYCLE

The RTE-VR4300-PC controls the bus cycle according to the type of device used (such as SRAM, DRAM, ROM, or I/O).   This section describes the timing of each access cycle.

5.3.1.   SRAM Access

SRAM access involves 0 to 3 wait states according to the setting of the PIO.   (See Section 5.2.2.)   Note that wait states can be inserted only in the read cycle.

SRAM Read Cycle (Swait[]=1)
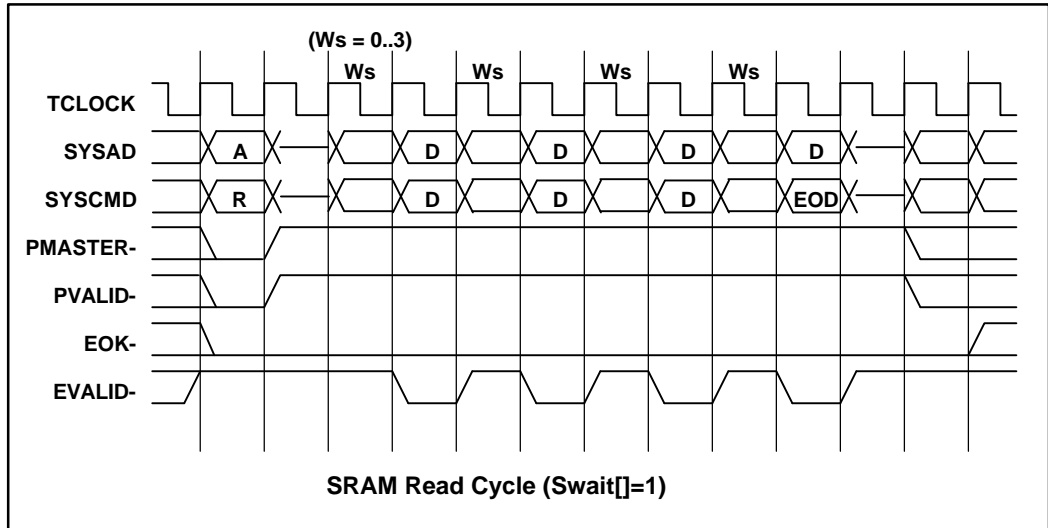
On the write cycle, latched data is written to SRAM always at the CPU data rate.

SRAM Write Cycle
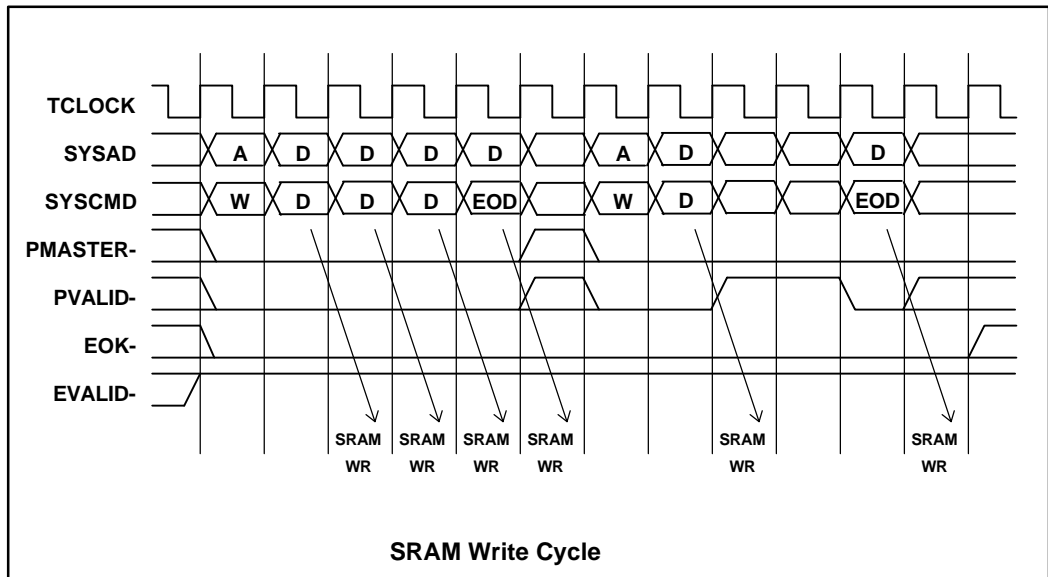
5.3.2.   DRAM Access

The RAS/CAS width and interleave/page hit can be controlled for DRAM according to the setting of the PIO.   (See Section 5.2.2.)

On a read cycle, data is latched on the positive-going edge of CAS, and EVALID- is returned on the next cycle.

DRAM Read Cycle (Dwid[]=1)
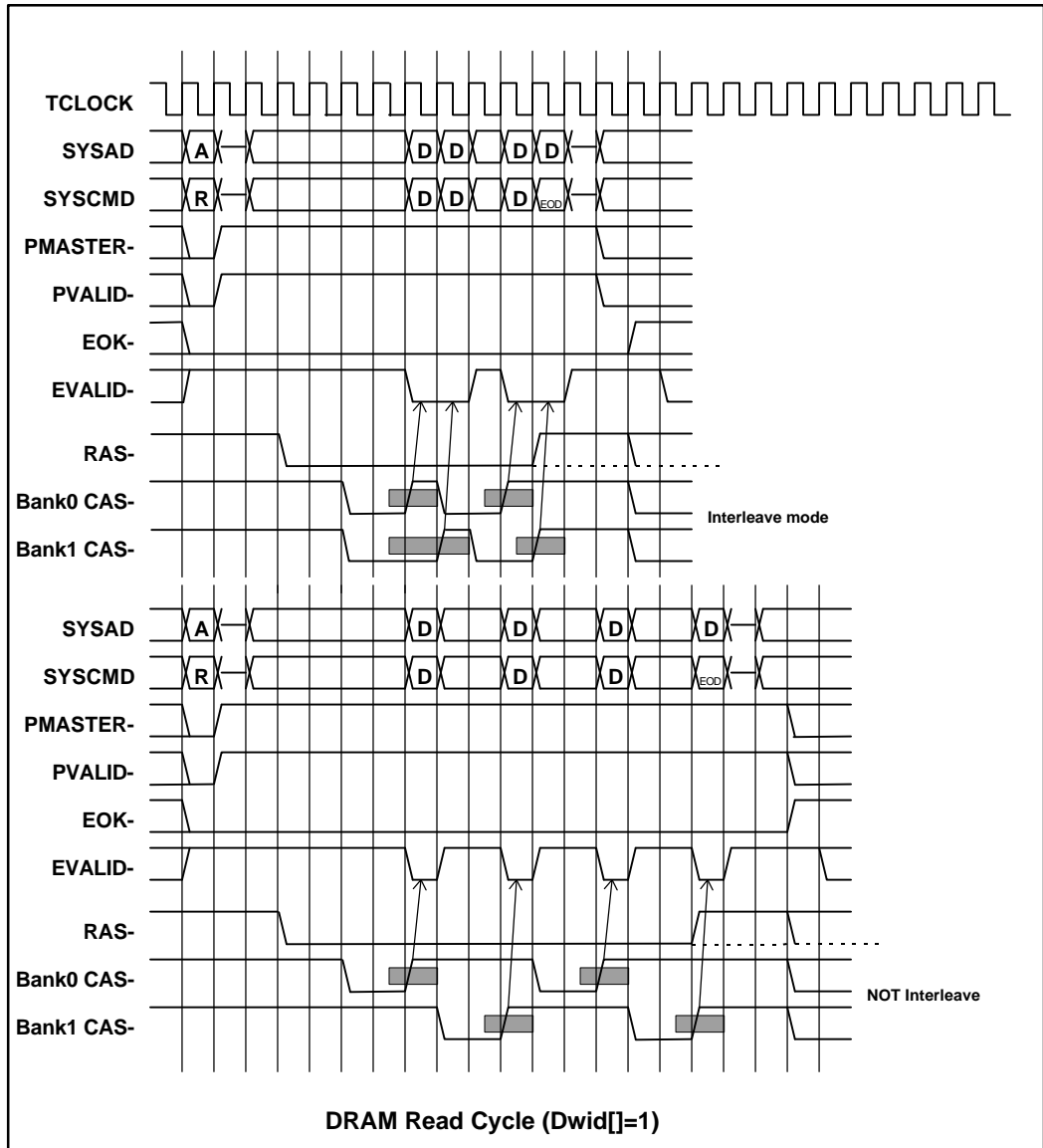
On the write cycle, EOK- is made negative, and the write data received from the CPU is saved in a register, then written to DRAM. After all data is written, EOK- is made positive again.

DRAM Write Cycle (Dwid[]=1, Data Rate=D)
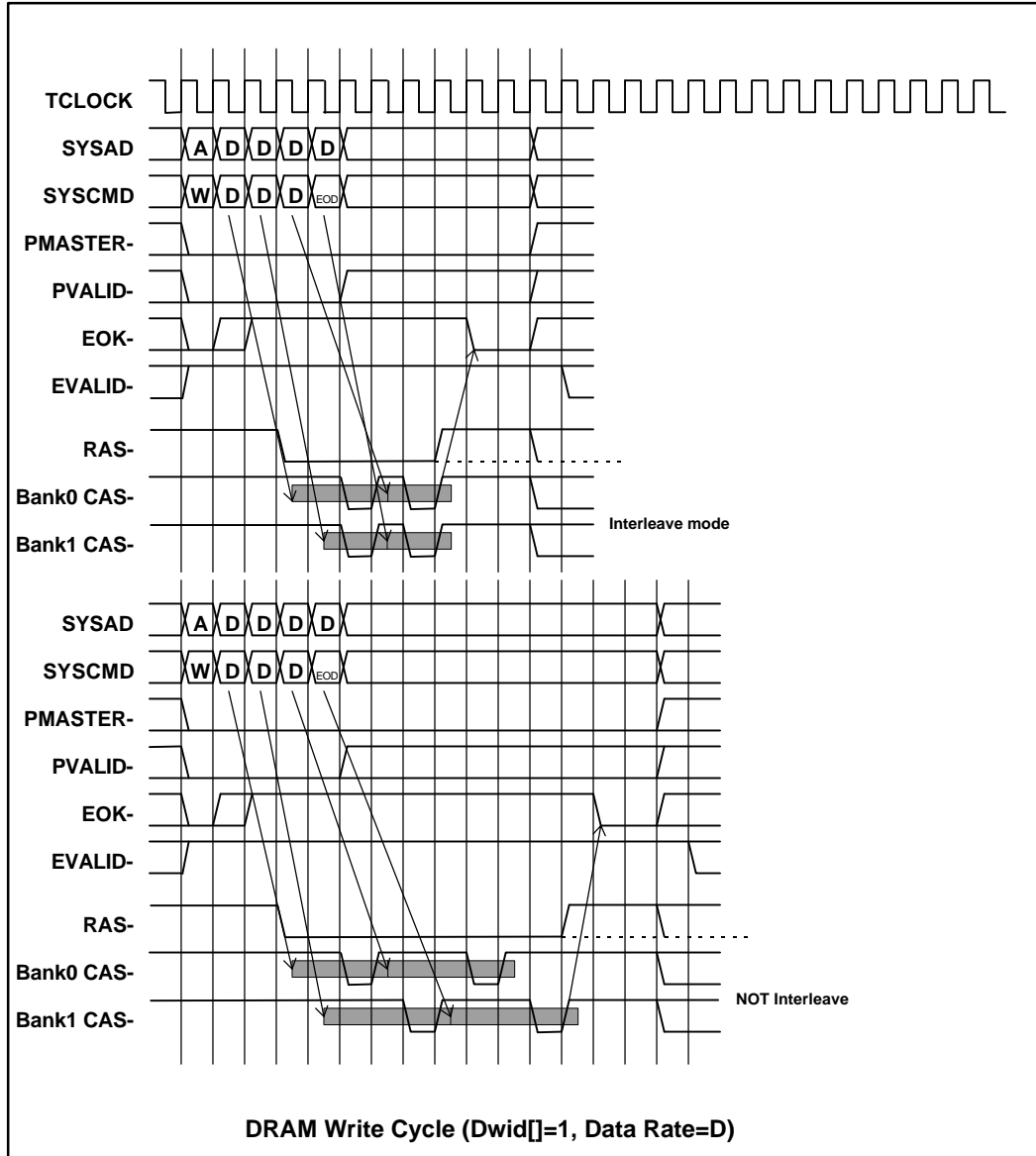
On the write cycle, CAS may be kept waiting if the data rate is not D (for example, if it is Dxx).

DRAM Write Cycle (Dwid[]=1, Data Rate=Dxx)
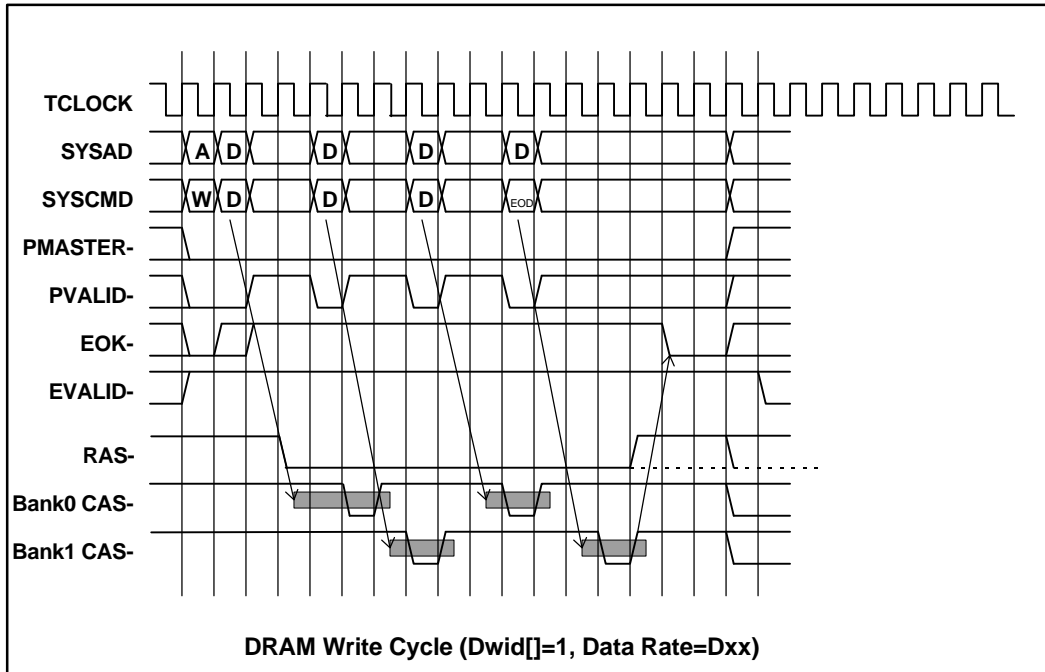
When the page hit mode is used, RAS is put on hold after DRAM access.   If the row address matches (hit) at the next access, the CAS cycle is executed immediately.   So, the number of access cycles used is reduced.   If a mismatch occurs (unhit), however, access is carried out on a usual RAS/CAS cycle after RAS precharge.   So overhead increases.

DRAM Page Hit/Unhit Cycle (Dwid[]=1)

CAS-before-RAS refresh is carried out for DRAM every 13 μs.

DRAM Refresh Cycle (Dwid[]=1)
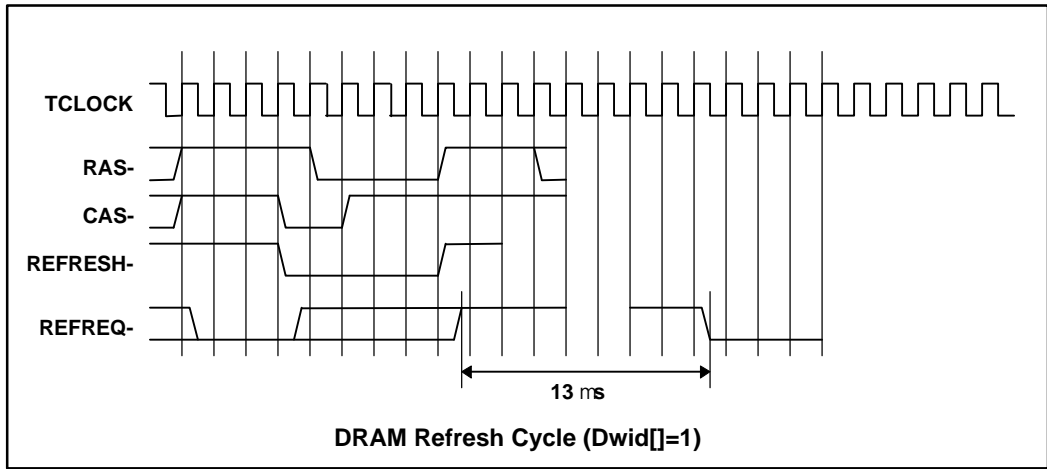
5.3.3. Local Bus Access

The local bus operates on a bus clock generated by dividing the frequency of the TCLOCK output from the CPU by 2.   It is used in accessing the ROM, I/O, and EXT-BUS units.   The minimum number of clock pulses for each cycle can be specified according to the PIO setting. (See Section 5.2.2.)

On a read cycle, data is latched on the positive-going edge of RD-, and EVALID- is returned on the next cycle.

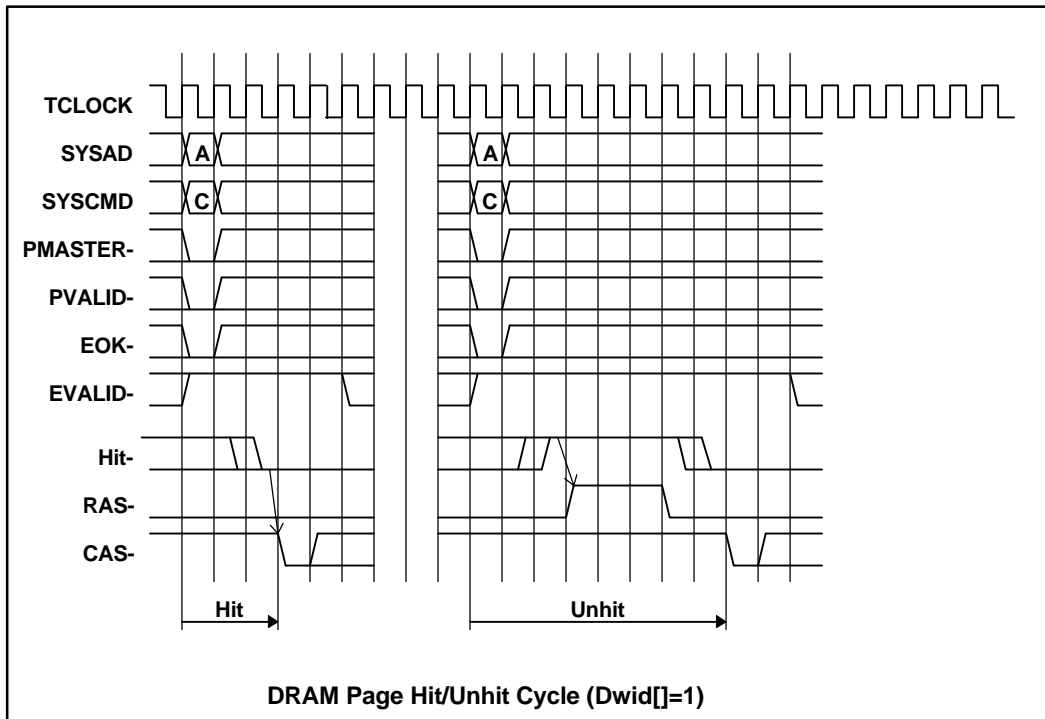On the write cycle, EOK- is made negative, and the CPU write data is saved in a register, then written to the local bus.   After all data is written, EOK- is made active again.

Local-BUS Cycles (Dwid[]=1)
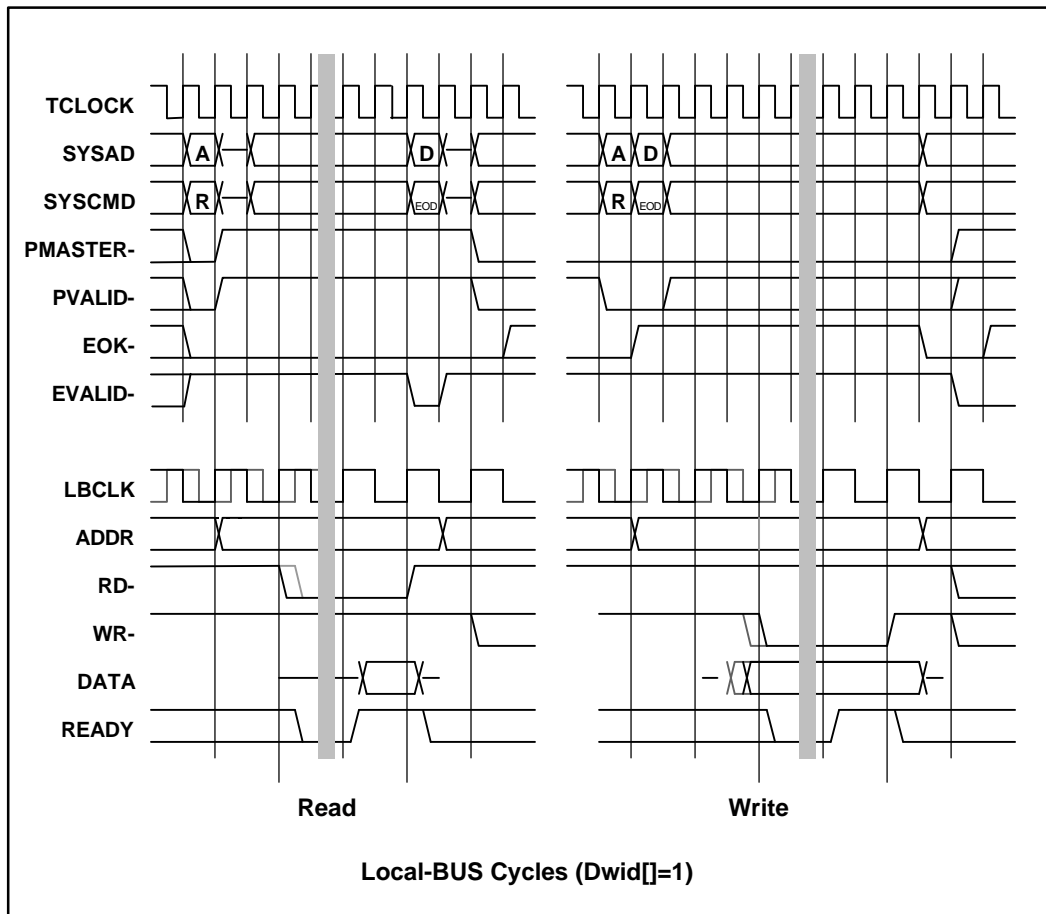
* The hatching at LBCLK, RD-, and WR- indicates a timing deviation due to the synchronization relationship between the TCLOCK and LBCLK.

The number of bus cycles involved is listed below.

Local bus device	Number of bus cycles (LBCLK)
ROM	4
SYSTEM-I/O	5
EXT-BUS	(Depending on READY)
TIMEOUT	256

Number of Local Bus Cycles

5.4. RESET

The factors listed below trigger a CPU reset.   These factors cold-reset the CPU.   They also system-reset the board control circuit.

- **Power-on reset**:   Occurs when the power to the board is switched on.
- **JP3 (ROMEM)-1**:   Input at the RESET pin of JP3.   (See Section 3.9.)
- **Reset switch**:   Generated by the reset switch (SWRESET) on the rear panel of the board.
- **Reset from the host**:   Sent via the ISA bus at the request of the host PC.

5.5. INTERRUPT

The interrupt sources outside the CPU are listed below.

Interrupt	Interrupt source
NMI-	JP3-3
INT0-	JP3-2, SCC2691 (serial/timer), ISA communication, TIMEOVER
INT1-	JP3-4
INT2-	JP3-6, EXT-BUS(INT-)
INT3-	JP3-8
INT4-	JP3-10

External Interrupts

Among the above interrupts, INT0 can be masked by hardware.   See description about IRQMASK in Section 5.2.2 for how to mask interrupts.

INT0 is handled according to the following procedure.

<1> Set the IRQMASK of the PIO to 1 to mask the interrupt by hardware.

<2> Check which has requested the interrupt (the ISR of the SCC2691, the TOVF- of the PIO, or any other).

<3> Handle the interrupt for the requester, and clear the request.

<4> Reset the IRQMASK of the PIO to 0, and unmask the interrupt.

<5> Exit the interrupt handling routine.

5.6. EXT-BUS SPECIFICATION

The EXT-BUS is used to expand memory and I/O units.   The local bus on this board is connected to the JEXT connector.

The following tables list the pin arrangement of the JEXT connector and the functions of each signal.   The timing relationships between the signals are also shown below.

Number	Signal name	Number	Signal name	Number	Signal name	Number	Signal name
1	**+5V**	2	**+5V**	31	**GND**	32	**GND**
3	D0	4	D1	33	A8	34	A9
5	D2	6	D3	35	A10	36	A11
7	D4	8	D5	37	A12	38	A13
9	D6	10	D7	39	A14	40	A15
11	**GND**	12	**GND**	41	**+5V**	42	**+5V**
13	D8	14	D9	43	A16	44	A17
15	D10	16	D11	45	A18	46	A19
17	D12	18	D13	47	BHE-	48	**GND**
19	D14	20	D15	49	**GND**	50	RD-
21	**+5V**	22	**+5V**	51	WR-	52	RESET-
23	A0	24	A1	53	**GND**	54	**GND**
25	A2	26	A3	55	READY	56	INT-
27	A4	28	A5	57	**GND**	58	**GND**
29	A6	30	A7	59	LBCLK	60	**GND**

JEXT Connector Pin Arrangement

Signal name	Input/ output	Function
+5V	-	Supply voltage of +5 V
GND	-	Ground
A[0..19]	Output	Address bus signal
BHE-	Output	Byte high enable signal, which is active when bits D[8..15] are enabled
D[0..15]	Input/ output	Data bus signal, which is originally the CPU data bus signal received at a buffer. It is pulled up with a 47 kΩ resistor on the board.
RD-	Output	Read cycle timing signal, which becomes active only when the EXT-BUS space is accessed.
WR-	Output	Write cycle timing signal, which becomes active only when the EXT-BUS space is accessed.
READY	Input	Signal indicating the end of a cycle. It is valid only for the EXT-BUS space. To have the CPU recognize READY securely, it is necessary to keep READY active until RD- or WR- becomes inactive. It is pulled up with a 10 kΩ resistor on the board.
INT-	Input	Active-low interrupt request signal, which is connected to the INT2-pin of the CPU via a buffer. It is pulled up with a 10 kΩ resistor on the board.
RESET-	Output	Active-low system reset signal
LBCLK	Output	Clock signal generated by dividing the frequency of the TCLOCK of the VR4300 by 2

JEXT Connector Signals
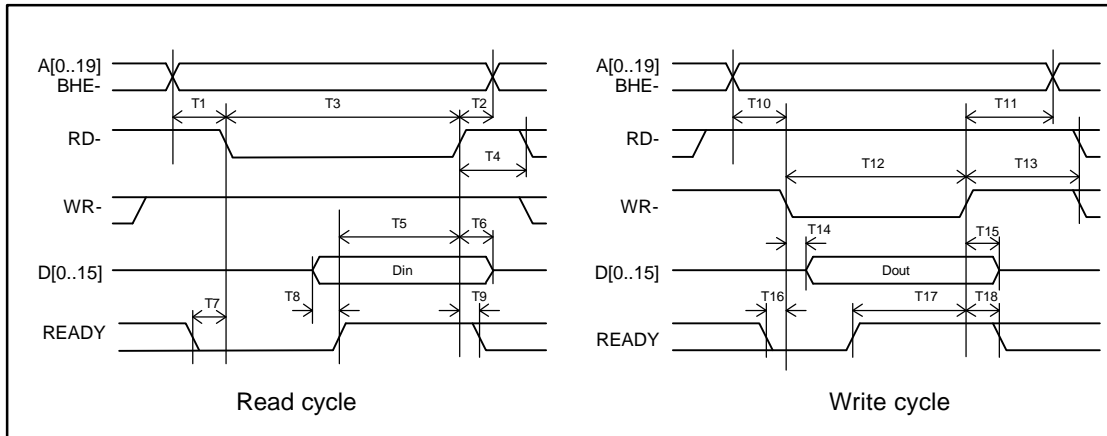
EXT-BUS Cycle

Symbol	Description	MIN(ns)	MAX(ns)
T1	RD address setup time	0	
T2	RD address hold-up time	0	
T3	RD cycle time	50	
T4	RD cycle interval	20	
T5	RD data setup time	15	
T6	RD data hold time	0	
T7	RD READY WAIT setup time	0	
T8	RD READY setup time	0	
T9	RD READY hold time	0	
T10	WR address setup time	0	
T11	WR address hold time	20	
T12	WR cycle time	50	
T13	WR cycle interval	20	
T14	WR data delay time		20
T15	WR data hold time	20	
T16	WR READY WAIT setup time	0	
T17	WR READY setup time	0	
T18	WR READY hold time	0	

EXT-BUS AC Specifications

6. Multi MONITOR

The ROM chip on the board is incorporated with the Multi monitor.   The following cautions should be observed when the board is connected to the Multi server as the host.

6.1. MONITOR WORK RAM

The monitor uses the SRAM area between the start address and 10000H (64 KB) as work RAM.   In other words, user programs are not allowed to use logical addresses 8000-0000H to 8000-FFFFH and A000-0000H to A000-FFFFH.

6.2. INTERRUPTS

When running on the Multi motor, user programs cannot use interrupts at present.

6.3. _INIT_SP SETTING

_INIT_SP (stack pointer initial value) is set to 8007-FFFCH (highest SRAM address) by the monitor.   (_INIT_SP can be changed in the Multi environment.)

6.4. REMOTE CONNECTION

Either serial or ISA bus connection can be selected for operation with the Multi server.   To switch from serial connection to ISA bus connection or vice versa, it is necessary to reset the monitor (by pressing the reset switch on the rear panel) and run the Check RTE utility of RTE for Windows.

7. RTE COMMANDS

When the monitor and MIDAS server (RTESERV) are connected with the Multi debugger, the TARGET window is opened.   The RTE commands can be issued in this window.   The following table lists the RTE commands.

Command	Description
HELP, ?	Displays help messages.
INIT	Initializes.
VER	Displays the version number.
CACHEFLUSH	Flushes the cache.
SHOWTLB	Displays the contents of the TLB.
IOREAD	Reads I/O data (with a size specified).
IOWRITE	Writes I/O data (with a size specified).

RTE Commands

Some commands require parameters.   All numeric parameters such as addresses and data are assumed to be hexadecimal numbers.   The following numeric representations are <u>invalid</u>:
0x1234, 1234H, $1234

7.1. HELP (?)

<Format>   HELP [command-name]

The HELP command displays a list of RTE commands and their formats.   A question mark (?) can also be used in place of the character string HELP.   If no command name is specified in the parameter part, the HELP command lists all usable commands.

<Example>   HELP INIT
Displays help messages for the INIT command.

7.2. INIT

<Format>   INIT

The INIT command Initializes the RTE environment.   Usually, this command should not be used.

7.3. VER

<Format>   VER

The VER command displays the version number of the current RTE environment.

7.4. CACHEFLUSH

<Format>   CACHEFLUSH

The CACHEFLUSH command flushes the contents of the cache in the CPU.

7.5. SHOWTLB

<Format>   SHOWTLB

The SHOWTLB command lists the contents of the TLB in the CPU.

7.6. IOREAD

<Format>   IOREAD   [BYTE│SHORT│LONG]   [address]

The IOREAD command reads memory at the specified address according to the specified size, and displays the data.   Select BYTE, SHORT, or LONG to specify 8, 16, or 32 bits.   Use this command to access memory mapped I/O.

<Example>   IOREAD   BYTE   BC000100
BC000100: 1A

7.7. IOWRITE

<Format>   IOWRITE   [BYTE│SHORT│LONG]   [data]   [address]

The IOWRITE command writes the specified data to memory at the specified address according to the specified size.   Select BYTE, SHORT, or LONG to specify 8, 16, or 32 bits. Use this command to access memory mapped I/O.

<Example>   IOWRITE   SHORT   30F0   BC00F000

8. APPENDIX

8.1. SWITCHES

• SW1

SW1 contact	Function
1	ON: Little endian OFF: Big endian (default)
2	Not used (fixed at OFF)
3	ON: DIVMODE0 = 0 (Low) OFF: DIVMODE0 = 1 (High)
4	ON: DIVMODE1 = 0 (Low) OFF: DIVMODE1 = 1 (High)
5	Not used (fixed at OFF)
6	Not used (fixed at OFF)
7	Not used (fixed at OFF)
8	ON: 64-bit monitor OFF: 32-bit monitor (default)

SW1 Setting

• SW2

SW2 contact	1	2	Baud rate
Setting	ON	ON	Not used
	OFF	ON	38400 baud
	ON	OFF	19200 baud
	OFF	OFF	9600 baud (factory-set)

Baud Rate Setting

SW2 contact	3	4	Profiler period
Setting	ON	ON	Timer interrupt is not used.
	OFF	ON	200 Hz 5ms
	ON	OFF	100 Hz 10ms
	OFF	OFF	60 Hz 16.67ms (factory-set)

Profiler Period Setting

SW2 contact	5	6	Data rate
Setting	x	ON	Dxx
	x	OFF	D (factory-set)

Data Rate Setting

• SW3

SW3 contact	1	2	3	4	5	6	7	8	
Address	A4	A5	A6	A7	A8	A9	A10	A11	I/O address
ON/ OFF	0	0	0	0	0	1	0	0	020xH (factory-set)

ISA-to-I/O Address Correspondence

8.2.   JUMPERS

• JP2 (SYNC)

JP2 connection	1-2	3-4	5-6	7-8	9-10	11-12
SYNC delay time	0ns	1ns (default)	2ns	3ns	4ns	5ns

JP2 Setting

• JP3 (ROMEMU)

JP3 pin	Function	JP3 pin	Function
1	RESET-input (active-low) 47 kΩ pull-up resistor	2	INT0-input (active-low) 47 kΩ pull-up resistor
3	NMI-input (active-low) 47 kΩ pull-up resistor	4	INT1-input (active-low) 47 kΩ pull-up resistor
5	Not used (NC)	6	INT2-input (active-low) 47 kΩ pull-up resistor
7	Not used (NC)	8	INT3-input (active-low) 47 kΩ pull-up resistor
9	Not used (NC)	10	INT4-input (active-low) 47 kΩ pull-up resistor
11	**GND**	12	**GND**

JP3 Functions

• JP4 (ROMSEL)

ROM type	Pin connection (with a bank)	Pin connection (with no bank)
271024 (64K x 16Bit)	9-10,11-12 (factory-set)	1-2, 3-4
272048 (128K x 16Bit)	-	1-2, 3-4, 5-6
274096 (256K x 16Bit)	-	1-2, 3-4, 5-6, 7-8

JP4 Pin Connection

- Memo -

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