RTE-VR5000-PC

USER' S MANUAL

Midas lab

REVISION HISTORY

Date Y	M	D	Rev	Description
96	11	12	1.00	First issue
99	4	10	1.01	Reviced *5.2 INTERRPUTS…INT2 <-> INT3

CONTENTS

1. INTRODUCTION

This manual describes the **RTE-VR5000-PC**, an evaluation board designed for use with the VR5000, NEC' s RISC CPU. The evaluation board consists of a VR5000 CPU capable of operating at up to 200 MHz, ROM (for booting), DRAM, and SRAM with a data bus width of 64 bits, and I/O devices such as two serial interfaces, a parallel interface, and timers.

ROM contains a monitor for Green Hills Software' s MULTI debugger, enabling program development/debugging in a MULTI environment. The corresponding socket can be used to connect a ROM emulator for evaluation purposes.

The evaluation board can be used for a range of purposes including processor performance evaluation, demonstration, simulation engine, and application program development.

1.1. NUMERIC NOTATION

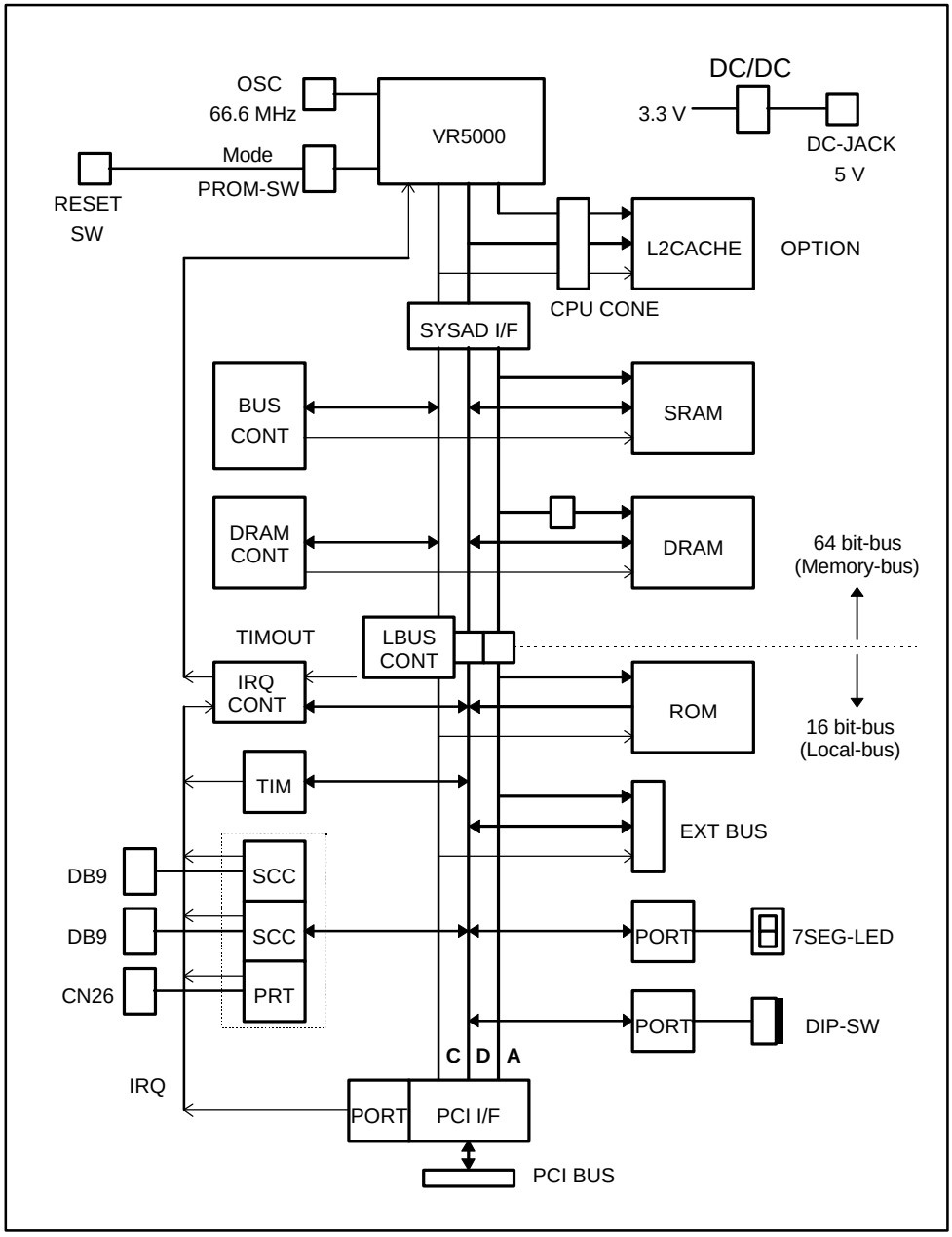
This manual represents numbers according to the notation described in the following table. Hexadecimal and binary numbers are hyphenated at every four digits, if they are difficult to read because of many digits being in each number. Letter x is used to represent an arbitrary numeral in a number, like " 1FxxH."

Number	Notation rule	Example
Decimal number	Only numerals are indicated.	" 10" represents number 10 in decimal.
Hexa-decimal number	A number is suffixed with letter H.	" 10H" represents number 16 in decimal.
Binary number	A number is suffixed with letter B.	" 10B" represents number 2 in decimal.

Number Notation Rules

2. FEATURES AND FUNCTIONS

The overview of each function block of the RTE-VR5000-PC is shown below:



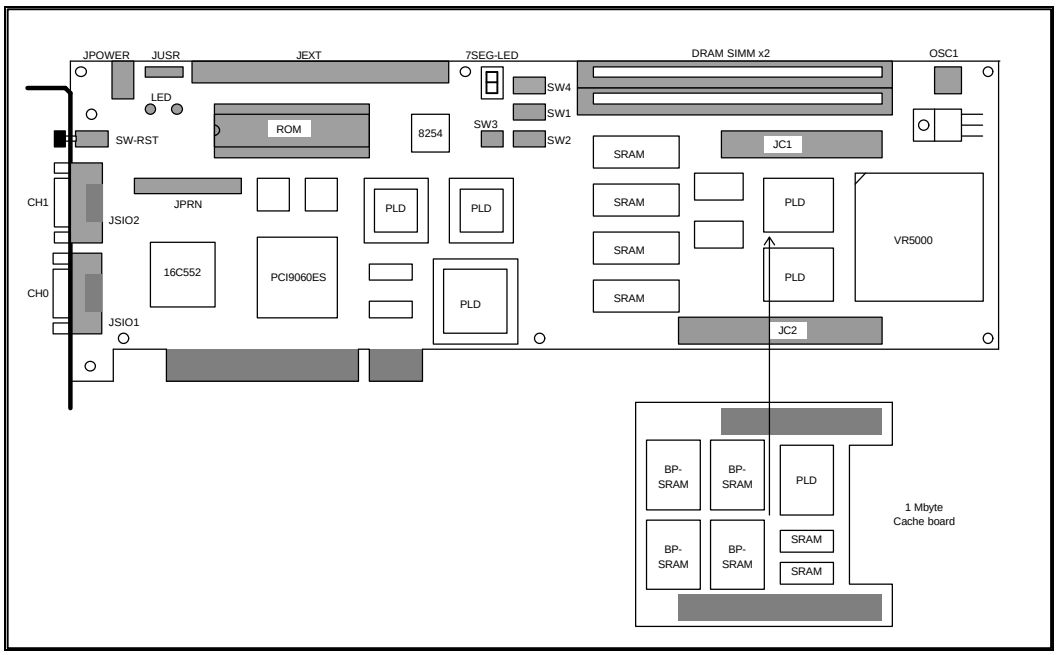
Block Diagram

Features

- ROM: 256 Kbytes (128K x 16 bits x 1)
- SRAM: 512 Kbytes (64K x 16 bits x 4)
- DRAM: 8, 16, or 32 Mbytes (standard of 8 Mbytes) installed in 72-pin SIMM sockets (x 2)
- RS-232C port x 2 ch (9-pin D-SUB connector)
- Parallel port of a PC/AT or compatible (male 26-pin header)
- Processor pin connector enabling measurement of all CPU signals (also used as cache connector)
- Connection pins for ROM in-circuit debugger

3. BOARD CONFIGURATION

The physical layout of the major components on the RTE-VR5000-PC board is shown below. This chapter explains each component.



Board Top View

3.1. RESET SWITCH (SW RST)

SW RST is a reset switch. Pressing this switch causes the CPU to be reset.

3.2. POWER SUPPLY CONNECTOR (JPOWER)

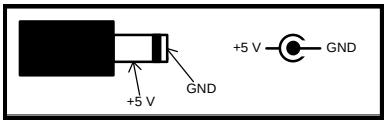
This jack-type connector is used to receive power from an external power supply. The JPOWER connector is rated as follows:

Voltage: 5 V

Current: Maximum of 4.0 A

Mating connector: Type A (5.5 mm in diameter)

Polarity:



[Caution] When attaching an external power supply to the board, be careful about its connector polarity.

3.3. LED INDICATORS

The following table lists the LED indicators and their meanings.

LED	Name	Meaning	Remark
LED1	TOVER	Indicates that a bus time-out has occurred.	For the local bus only
LED2	POWER	Indicates that the power is on.	
U36	-	7-segment LED (for port output)	

The 7-segment LED indicator can be turned on and off according to the data at the general-purpose output port. See Section 5.4.3 for details.

3.4. CPU-MODE SWITCHES (SW1 AND SW2)

SW1 and SW2 are switches for setting the operation mode of the CPU. The settings of the switches are used as data to be set at the MODEIN terminal at a cold reset. For these switches, the OFF position corresponds to logical 1, while the ON position corresponds to logical 0. See Section 4.1 for details.

3.5. ROM BANK SWITCH (SW3)

SW3 is a switch for setting the ROM banks. It controls the two high-order bits of the ROM address, specifying up to four banks, each having up to 64 Kbytes of space. See Section 4.1 for details of bank setting.

ROM address (16 bits)	Bank	Use (MULTI monitor)
0x00000-x07FFF	Bank 0	For little endian/64 bits
0x08000-x0FFFF	Bank 1	For big endian/64 bits
0x10000-x17FFF	Bank 2	For little endian/32 bits
0x18000-x1FFFF	Bank 3	For big endian/32 bits

3.6. GENERAL-PURPOSE INPUT SWITCH (SW4)

SW4 is a switch for setting data in the general-purpose input port. For this switch, the OFF position corresponds to logical 1, while the ON position corresponds to logical 0. See Sections 4.1 and 5.4.3 for details.

3.7. USER CONTROL PIN (JUSR)

The JUSR connector is a control terminal, mainly used with the ROM in-circuit debugger. It enables the input of reset and interrupt signals from the ROM in-circuit debugger.

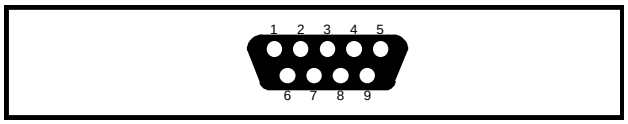
JROMEN	Name	Function	Remark
1	RST	RESET- input (active-low)	10 kΩ pull-up resistor
2	NMI	NMI- input (active-low)	10 kΩ pull-up resistor
3	IRQ	INT3- input (active-low)	10 kΩ pull-up resistor
4	GND	Ground	

3.8. CPU TEST CONNECTORS (JC1 AND JC2)

The JC1 and JC2 connectors are connected to the CPU pins. They are used for signal measurement and for connection to an optional cache board. See Section 9.1 for details of the pin arrangement of these connectors.

3.9. SERIAL CONNECTORS (JSIO1 AND JSIO2)

JSIO1 and JSIO2 are RS-232C connectors controlled by the serial/parallel controller (TL16C552A). They are 9-pin male D-SUB connectors usually used on the PC/AT. All signals on these connectors are on the RS-232C level. The following table lists the connector pin numbers and their functions. The table also lists the pin arrangement of the host machine' s 9-pin and 25-pin D-SUB connectors which are connected to the cable attached to JSIO1 or JSIO2. This cable is a cross-connection cable.



Pin Arrangement of JSIO1 and JSIO2

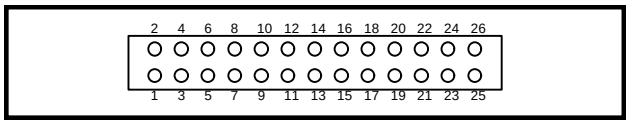
JSIOx pin	Signal name	Input/output	Pin arrangement on the host side	
			D-SUB9	D-SUB25
1	DCD	Input		
2	RxD (RD)	Input	3	2
3	TxD (SD)	Output	2	3
4	DTR (DR)	Output	1, 6	6, 8
5	GND		5	7
6	DSR (ER)	Input	4	20
7	RTS (RS)	Output	8	5
8	CTS (CS)	Input	7	4
9	RI	Input		

JSIO1 and JSIO2 Connector Signals

[Memo] On the panel, JSIO1 and JSIO2 are indicated as " CH0" and " CH1" respectively.

3.10. PARALLEL CONNECTOR (JPRT)

JPRT is a connector for a printer controlled by the serial/parallel controller (TL16C552A). This connector has 26 header pins, so a conversion cable is necessary if it is to be used as a typical printer connector. Its pin arrangement is shown below:



JPRT Pin Arrangement

JPRT pin	Signal name	Input/output	Remark
1	STB-	Output	10 kΩ pull-up resistor
2	AUTO_FD-	Output	10 kΩ pull-up resistor
3	D0	Output	10 kΩ pull-up resistor
4	ERROR-	Input	10 kΩ pull-up resistor
5	D1	Output	10 kΩ pull-up resistor
6	INIT-	Output	10 kΩ pull-up resistor
7	D2	Output	10 kΩ pull-up resistor
8	SELECT_IN-	Output	10 kΩ pull-up resistor
9	D3	Output	10 kΩ pull-up resistor
11	D4	Output	10 kΩ pull-up resistor
13	D5	Output	10 kΩ pull-up resistor
15	D6	Output	10 kΩ pull-up resistor
17	D7	Output	10 kΩ pull-up resistor
19	ACK-	Input	10 kΩ pull-up resistor
21	BUSY	Input	10 kΩ pull-up resistor
23	PE	Input	10 kΩ pull-up resistor
25	SELECT	Input	10 kΩ pull-up resistor
26	NC		Not used
10,12,14,16, 18,20,22,24	GND		

JPRT Connector Signals

3.11. OSCILLATOR SOCKET (OSC1)

OSC1 is an oscillator socket used to supply clock pulses to the CPU. A 66.6 MHz oscillator is factory-installed in the socket.

[Caution] Be careful when cutting the oscillator pins prior to installation. If a pin is too short, the oscillator housing may touch the socket pin, causing a short-circuit.

3.12. DRAM-SIMM SOCKET

The DRAM-SIMM socket is fitted with a 4-Mbyte SIMM as standard. This socket can be used to install a 4-, 8-, or 16-Mbyte 72-pin SIMM (for so-called DOS/V machines), such that the amount of installed DRAM can be increased. The type of SIMM currently installed can be detected from the I/O port. (See Section 5.4.2.)

3.13. ROM SOCKET

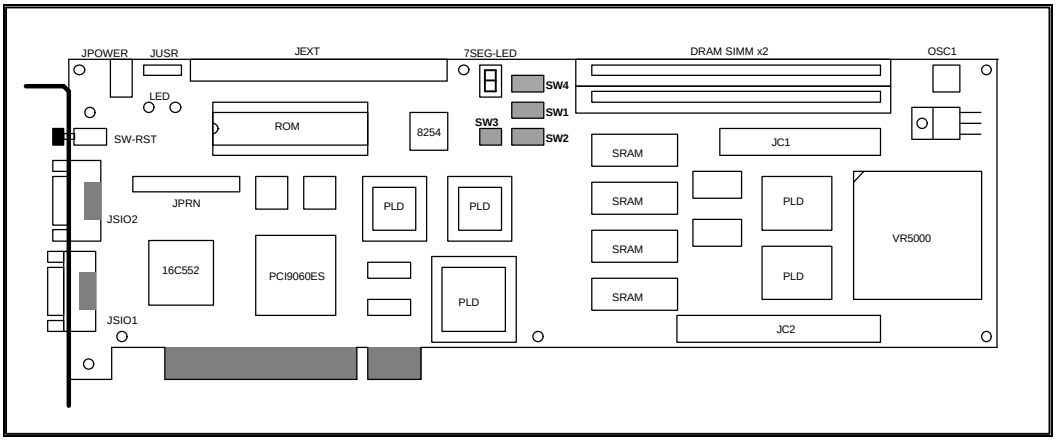
The ROM socket is fitted with a 40-pin 256-Kbyte (128K x 16) ROM chip as standard. The access time for this ROM should be 150 ns or less. The ROM can have up to four banks, selected by address switching, to support different endian and operation modes. See Sections 3.5 and 4.1 for an explanation of bank setting.

4. INSTALLATION AND USE

This chapter explains how to set the switches on the evaluation board, assuming that the board is to be used with the MULTI debugger. For an explanation of how to install the MULTI debugger on the host machine, refer to the manual supplied with the debugger. To connect a ROM emulator to the evaluation board, refer to the applicable manual for the emulator.

4.1. SWITCH SETTING

The evaluation board is equipped with several DIP switches. Their locations are as shown below:



Switches on the Evaluation Board

SW1 and SW2 are used to specify the operation mode, endian mode, and internal clock of the CPU.

SW1				Write data rate (XmitDatPat)	Remark (The asterisk indicates the factory-setting.)
1	2	3	4		
ON	ON	ON	ON	0: DDDD	**Unusable**
ON	ON	ON	OFF	1: DDxDDx	**Unusable**
ON	ON	OFF	ON	2: DDxxDDxx	
ON	ON	OFF	OFF	3: DxDxDxDx	*
ON	OFF	ON	ON	4: DDxxxDDxxx	
ON	OFF	ON	OFF	5: DDxxxxDDxxxx	
ON	OFF	OFF	ON	6: DxxDxxDxxDxx	
ON	OFF	OFF	OFF	7: DDxxxxxDDxxxxx	
OFF	ON	ON	ON	8: DxxxDxxxxDxxxDxxxx	
Miscellaneous				9-15: Reserved	Reserved

SW1			Processor clock (SysCkRatio)	Remark (The asterisk indicates the factory-setting.)
5	6	7		
ON	ON	ON	0: SysClock x 2	
ON	ON	OFF	1: SysClock x 3	*
ON	OFF	ON	2: SysClock x 4	
ON	OFF	OFF	3: SysClock x 5	
OFF	ON	ON	4: SysClock x 6	
OFF	ON	OFF	5: SysClock x 7	
OFF	OFF	ON	6: SysClock x 8	
OFF	OFF	OFF	7: Reserved	Reserved

SW1	Endian (EndBit)	Remark (The asterisk indicates the factory-setting.)
8		
ON	0: Little endian	
OFF	1: Big endian	*

SW2		Write mode (Nonblock Write)	Remark (The asterisk indicates the factory-setting.)
1	2		
ON	ON	0: R4x00 compatible	*
ON	OFF	1: Reserved	Reserved
OFF	ON	2: Pipeline write	**Unusable**
OFF	OFF	3: Write retry	

SW2	INT5 timer interrupt (TmrIntEn)	Remark (The asterisk indicates the factory-setting.)
3		
ON	0: Enable	*
OFF	1: Disable	

SW2	Secondary cache (Secondary Cache Enable)	Remark
4		
ON	0: Disable	With no cache board
OFF	1: Enable	With a cache board

SW2		Output drive setting (DrvOut)	Remark (The asterisk indicates the factory-setting.)
5	6		
ON	ON	0: 67 %	
ON	OFF	1: 50 % (slowest)	
OFF	ON	2: 100 % (fastest)	*
OFF	OFF	3: 83 %	

SW2		Secondary cache size (Secondary Cache Size)	Remark (The asterisk indicates the factory-setting.)
7	8		
ON	ON	0: 512 Kbytes	
ON	OFF	1: 1 Mbyte	*
OFF	ON	2: 2 Mbytes	
OFF	OFF	3: Reserved	Reserved

SW3 is a switch for ROM bank setting.

SW3 1	32-/64-bit operation (MD32/64)	Remark (The asterisk indicates the factory-setting.)
ON	0: 64-bit mode	
OFF	1: 32-bit mode	*

SW3		ROM address		Bank selection (The asterisk indicates the factory-setting.)
2	3	ROM-A15	ROM-A16	
ON	ON	CPU-A16	CPU-A17	No bank
ON	OFF	CPU-A16	ENDIAN	Endian only
OFF	ON	CPU-A16	MD32/64	Operation bit mode only
OFF	OFF	ENDIAN	MD32/64	Full-bank*

SW3 4	(Not used)	Remark (The asterisk indicates the factory-setting.)
OFF		*

SW4 is a switch for the general-purpose input/output port. The MULTI monitor in the installed ROM uses this switch to specify the baud rate for the RS-232C interface and the timer period of the profiler.

SW4		Baud rate (JSIO1)	Remark (The asterisk indicates the factory-setting.)
1	2		
ON	ON	0: 115.2K bps	
OFF	ON	1: 38400 bps	
ON	OFF	2: 19200 bps	
OFF	OFF	3: 9600 bps	*

[Memo] The other communication settings are fixed as follows: 8 data bits, no parity, and one stop bit

SW4		MULTI profiler period (timer 0)	Remark (The asterisk indicates the factory-setting.)
3	4		
ON	ON	0: No profiler is used.	There is no interrupt timer.
OFF	ON	1: 200 Hz 5.0 ms	
ON	OFF	2: 100 Hz 10.0 ms	
OFF	OFF	3: 60 Hz 16.67 ms	*

Circuits 5 to 8 of SW4 are not used by the MULTI monitor; they are always kept in the OFF position.

4.2. CONNECTION WITH THE HOST MACHINE

4.2.1. Standalone Use of the Evaluation Board (Connection via RS-232C)

To connect the evaluation board to the host machine, follow the procedure given below.

<1> Prepare an RS-232C cable for connection with the host. Also, prepare an external power supply (+5 V, 4 A). For the power supply, especially, pay particularly careful attention to its voltage and **connector polarity**. See Section 3.9 for an explanation of how to attach the RS-232C cable and Section 3.2 for details of the power supply connector.

<2> Connect the host machine to the JSIO1 (CH0) connector via an RS-232C cable, supply power to the evaluation board from the JPOWER connector, and check that the POWER-LED on the evaluation board is lit. **If the LED is not lit, switch off the power and disconnect the evaluation board immediately.**

<3> Start the MULTI debugger on the host machine to establish a connection via the RS-232C interface. If an error occurs, check the serial cable connection and switch settings (especially the baud rate).

[Caution] When power is supplied, the CPU and heat sink become hot. They remain hot for a while after the power is switched off. Be careful not to touch them while they are hot.

4.2.2. Incorporation of the Evaluation Board in the PCI Slot (Connection via the PCI Bus)

To incorporate the evaluation board in the PCI slot of the host machine, follow this procedure.

<1> Open the cabinet of the host machine and install the evaluation board in the PCI slot. Check that it is firmly seated, then tighten the screw to fasten the back panel.

<2> Switch on the power of the host machine, and check whether the POWER-LED on the evaluation board is lit. **If the LED is not lit, switch off the power and disconnect the evaluation board immediately.** Also, check whether the host machine can be started normally.

<3> Start the MULTI debugger on the host machine to establish a connection via the PCI bus. If an error occurs, check the board and software installation.

[Memo] If Windows 95 is used on the host PC, when the evaluation board is incorporated and Windows 95 is activated, Windows 95 displays a dialog box to prompt you to install the PCI driver. In the menu of this dialog box, install the driver according to the following procedure:

- Select from the driver list
- Other devices
- Unsupported devices

In addition, if you subsequently remove the evaluation board, uninstall the driver.

5. HARDWARE REFERENCE

This chapter describes the hardware functions of the RTE-VR5000-PC board.

5.1. RESET

The following factors cause a reset. This reset is treated as a cold reset by the CPU and is used as a system reset for the control circuits on the evaluation board.

- **Power-on reset**: Occurs when power to the evaluation board is applied.
- **Reset switch**: Occurs when the reset switch (SW RST) on the evaluation board is pressed.
- **Host reset**: Requested by the host PC via the PCI bus controller.
- **JUSR-1**: Input from pin 1 (RST) of the JUSR connector (See Section 3.7).

5.2. INTERRUPTS

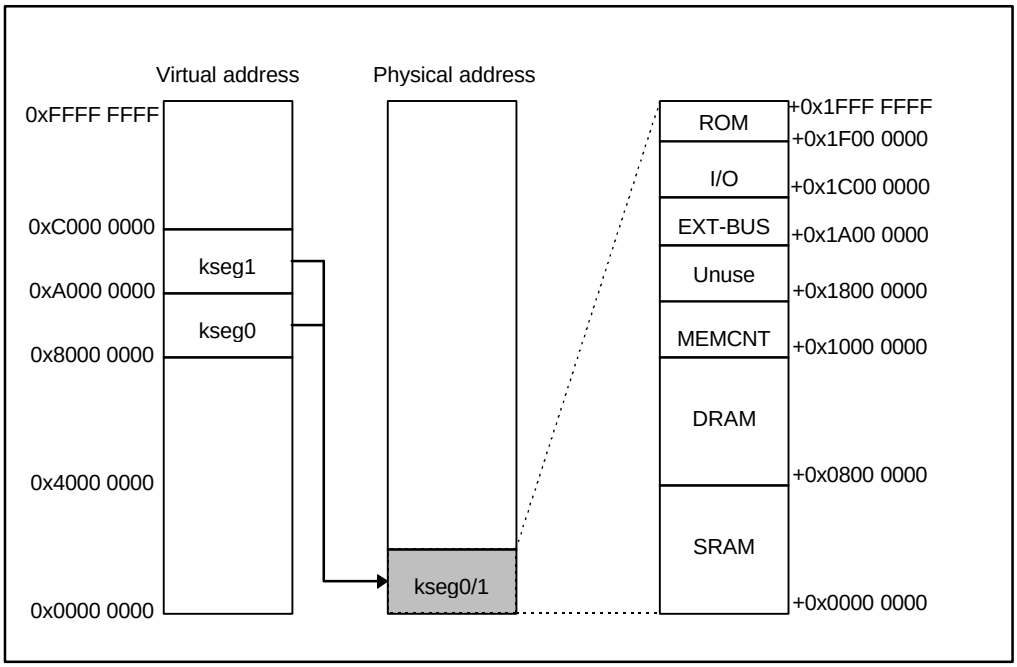
The following table lists interrupt sources external to the CPU.

Interrupt	Source	Reference
NMI-	JUSR-2(NMI)	Section 3.7
INT0-	Interrupt controller INT0M	Section 5.4.6
INT1-	Interrupt controller INT1M	Section 5.4.6
INT2-	EXT-BUS	Section 5.6
INT3-	JUSR-3 (IRQ)	Section 3.7
INT4-	Not used (fixed to 1)	
INT5-	Not used (internal CPU timer)	

The external interrupts can be masked by hardware. (See Section 5.4.6.)

5.3. ADDRESS MAP

The address assignment of the evaluation board is shown below:



Address Map

With the MULTI monitor, programs are executed in the kernel address space (8000-0000H to BFFF-FFFFH), in which no TLB map is used. The logical address of the address space is obtained by adding 8000-0000H (if a cache is used) or A000-0000H (if no cache is used) to the physical address.

5.3.1. SRAM Address Space (0000-0000H to 07FF-FFFFH)

The SRAM on the evaluation board has 512 Kbytes of real address space. Other addresses constitute an image address space. If the frequency of the external bus clock is 40 MHz or higher, it is necessary to insert at least one wait state into the SRAM access cycle, using the SRAM controller (SRAMC). (See Section 5.4.1.) This address space can be accessed as either a cache or noncache space.

5.3.2. DRAM Address Space (0800-0000H to 0FFF-FFFFH and x800-0000H to xFFF-FFFFH)

The DRAM address space is implemented as a 72-pin DRAM-SIMM, installed on the evaluation board. The evaluation board is equipped with a 4-Mbyte SIMM as standard. It can be replaced with an 8-Mbyte or 16-Mbyte SIMM for memory expansion. In addition to the two installed DRAM-SIMMs, an image address space is available. The DRAM access timing is set using the DRAM controller (DRAMC). (See Section 5.4.2.) This address space can be accessed as either a cache or noncache space.

5.3.3. MEM-CNT Address Space (1000-0000H to 17FF-FFFFH)

The SRAM and DRAM access control registers are mapped onto the MEM-CNT address space. See Sections 5.4.1 and 5.4.2 for details. This address space can be accessed as a noncache space.

5.3.4. Unused Space (1800-0000H to 19FF-FFFFH)

If a time-out function is enabled, accessing this address space forcibly terminates the bus cycle when a time-out delay occurs, thus generating a time-out interrupt.

5.3.5. EXT-BUS Address Space (1A00-0000H to 1BFF-FFFFH)

The EXT-BUS address space is a 1-Mbyte real address space for the EXT-BUS external enhanced bus. The remaining space functions as an image address space. The EXT-BUS address space can be accessed as a noncache space.

5.3.6. I/O Address Space (1C00-0000H to 1EFF-FFFFH)

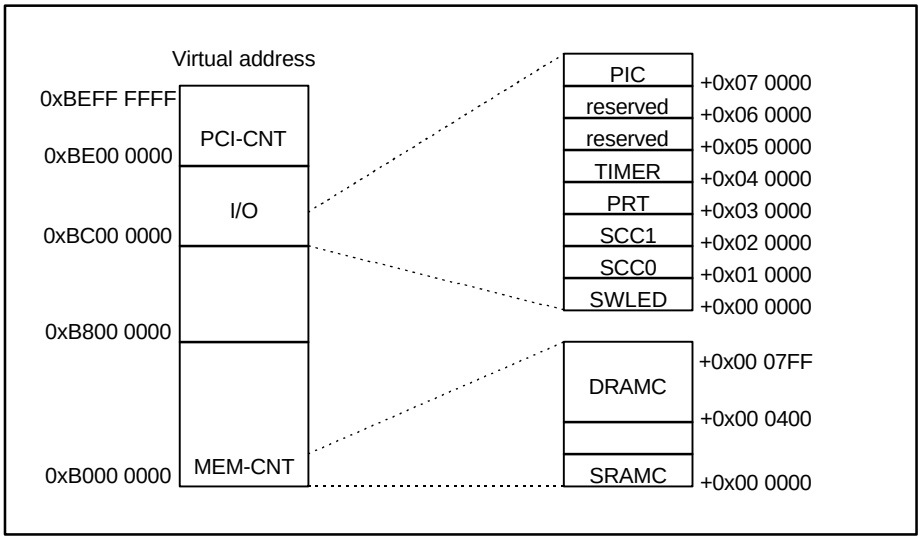
The I/O address space is an address space (memory mapped I/O) allocated to those I/O devices that control functions on the evaluation board. See Section 5.4 for details of I/O mapping. The I/O address space can be accessed as a noncache space.

5.3.7. ROM Address Space (1F00-0000H to 1FFF-FFFFH)

The ROM address space is a 256-Kbyte (272048) real address space in ROM of the evaluation board. The remaining space functions as an image address space. The factory-installed ROM holds the MULTI monitor. The ROM address space can be accessed as a noncache space.

5.4. DETAILS OF I/O DEVICES

The memory-mapped I/O devices include a memory access controller, DUART/LPT, timer, interrupt controller, and PCI (communication I/O) controller. They are memory-mapped as shown below:



I/O Map

These I/O devices are designed for access to the kernel noncache address space, so the following descriptions focus on their use with the logical address.

[Memo] Unless otherwise stated, the I/O devices are connected to D[7..0] of the data bus. It is therefore necessary to be aware of the endian mode during byte access. For byte access to data in big endian mode, it is necessary to add 7 as a byte offset.

5.4.1. SRAM Controller (SRAMC)

The SWAIT register is used to control the wait states for the SRAM address space. With this register, it is possible to insert 0 to 3 wait states in the read cycle. The register assignment for the SRAM controller is listed below:

Logical address	Register	Data bus			
		D3	D2	D1	D0
B000-0000H	**SRAMC SWAIT**	0	0	SWAIT1	SWAIT0

SWAIT[1..0]: Specify the number of wait states used when reading from SRAM.

SWAIT		Number of wait states in SRAM read
1	0	
0	0	0
0	1	1
1	0	2
1	1	3 (Reset value)

[Memo] 0 wait state can be specified for SRAM only when the frequency of the external bus block (SysClock) is 40 MHz or lower, that is, when one clock period is 25 ns or longer. This condition is determined by:

Address delay + SRAM access time + data setup =

5 ns + 17 ns + 3 ns = 25 ns

5.4.2. DRAM Controller (DRAMC)

The DRAMC is used to control access to DRAM. Its registers are set with RAS/CAS widths and operation modes. The register assignment for the DRAM controller is as listed below:

Logical address	Register	Data bus			
		D3	D2	D1	D0
B000-0400H	**DRAMC RCAS**	0	0	RCAS1	RCAS0
-0500H	**DRAMC MRAS**	0	MRAS2	MRAS1	MRAS0
-0600H	**DRAMC PRAS**	0	PRAS2	PRAS1	PRAS0
-0700H	**DRAMC DMODE**	PD1	PD2	EDOEN	HITEN

RCAS[1..0]: Specify the number of clock cycles for the DRAM CAS read cycle. The actual number of clock cycles is the specified value (0 to 3) plus 1.

RCAS		Number of CAS read cycles
1	0	
0	0	1 SYSCLK
0	1	2 SYSCLK
1	0	3 SYSCLK
1	1	4 SYSCLK (Reset value)

[Memo] The CAS precharge cycle is fixed to one clock cycle.

MRAS[2..0]: Specify the number of clock cycles for the DRAM RAS access cycles. The actual number of cycles is the specified value (0 to 7) plus 1.

MRAS			Number of RAS access cycles
2	1	0	
0	0	0	1 SYSCLK
0	0	1	2 SYSCLK
0	1	0	3 SYSCLK
0	1	1	4 SYSCLK
1	0	0	5 SYSCLK
1	0	1	6 SYSCLK
1	1	0	7 SYSCLK
1	1	1	8 SYSCLK (Reset value)

PRAS[2..0]: Specify the number of DRAM RAS precharge cycles. The actual number of cycles is the specified value (0 to 7) plus 1.

PRAS			Number of RAS precharge cycles
2	1	0	
0	0	0	1 SYSCLK
0	0	1	2 SYSCLK
0	1	0	3 SYSCLK
0	1	1	4 SYSCLK
1	0	0	5 SYSCLK
1	0	1	6 SYSCLK
1	1	0	7 SYSCLK
1	1	1	8 SYSCLK (Reset value)

HITEN: Specifies whether to use the page hit access function of the DRAM controller. When HITEN = 1, high-speed page access is implemented if the RAS held at the end of DRAM access matches the row address (DRAM page address) during the next DRAM access. The RAS cycle is released from hold by a refresh request. If no hit occurs, normal access is performed after the precharge cycle.

HITEN	DRAM page hit
0	Not to be used (Reset value)
1	To be used

EDOEN: Specifies whether DRAM is of FPM or EDO type. When EDOEN = 1, the CAS width may be able to be reduced by one clock cycle, because a data delay during burst read coincides with the CAS precharge period.

EDOEN	DRAM type
0	FPM-DRAM (Reset value)
1	EDO-DRAM

PD[1..2]: Enable reading of the DRAM-SIMM type terminal PD[1..2] (read-only).

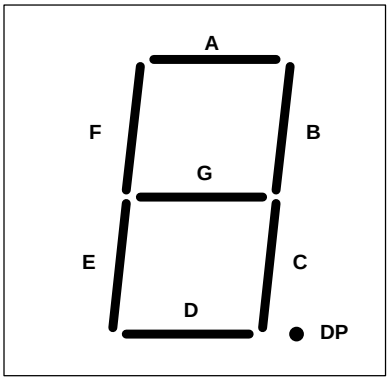
PD1	PD2	DRAM-SIMM capacity
0	0	4 Mbytes (Standard)
0	1	16 Mbytes
1	0	(Reserved)
1	1	8 Mbytes

5.4.3. General-Purpose Input/Output Port (SWLED)

The general-purpose input/output port controls the reading of the settings of the DIP switch (SW4) and the indication of the 7-segment LED indicator on the evaluation board.

Logical address	Data bus								Contents
	D7	D6	D5	D4	D3	D2	D1	D0	
BC00-0000H Input	SW4 -8	SW4 -7	SW4 -6	SW4 -5	SW4 -4	SW4 -3	SW4 -2	SW4 -1	**0=ON** 1=OFF
BC00-0000H Output	7SEG -DP	7SEG -G	7SEG -F	7SEG -E	7SEG -D	7SEG -C	7SEG -B	7SEG -A	**0 = ON** 1 = OFF

The correspondence between the data bus bits and LED segments is as shown below:



[Caution] It is impossible to read data output to the 7-segment LED indicator.

5.4.4. Serial/Parallel I/O Device (SCC0/1 and LPT)

The serial/parallel I/O device is TI' s TL16C552A. This device incorporates two NS16550-compatible serial controllers and a PC/AT (PS2)-compatible parallel port. The register assignment for the TL16C552A is as listed below:

Logical address	Register	Supplement
BC01-0000H	RBR/THR/DLL	SCC0
-0100H	IER/DLM	
-0200H	IIR/FCR	
-0300H	LCR	
-0400H	MCR	
-0500H	LSR	
-0600H	MSR	
-0700H	SCR	
BC02-0000H	RBR/THR/DLL	SCC1
-0100H	IER/DLM	
-0200H	IIR/FCR	
-0300H	LCR	
-0400H	MCR	
-0500H	LSR	
-0600H	MSR	
-0700H	SCR	
BC03-0000H	LPD	LPT
-0100H	LPS	
-0200H	LPC	
-0300H	-	

The input clock frequency for the serial controller is 16 MHz. Refer to the manual provided with the TL16C552A for an explanation of the functions of each register.

5.4.5. Timer

The timer is NEC' s μPD71054. The μPD71054 is compatible with Intel' s i8254. This timer has three counters. These counters are used to realize various types of control.

Each register of the μPD71054 is allocated addresses as listed below:

Logical address	Register	Supplement
BC04-0000H	PCNT0	Timer 0
-0100H	PCNT1	Timer 1
-0200H	PCNT2	Timer 2
-0300H	PCNTL	Control

Refer to the manual provided with the μPD71054 or i8254 for an explanation of the functions of each register.

The timers are used as listed below:

Timer	Clock	Mode	Use	
0	2 MHz	2	Timer interrupt 0	Used by the monitor
1	2 MHz	2	Timer interrupt 1	Usable by the user
2	2 MHz	2	DRAM refresh	

5.4.6. Interrupt Controller (PIC)

The PIC is mainly used to control interrupts. The register assignment for the PIC is as listed below:

Logical address	Register	Data bus							
		D7	D6	D5	D4	D3	D2	D1	D0
BC07-0000H	**PIC INT0M**	IM07	IM06	IM05	IM04	IM03	IM02	IM01	IM00
-0100H	**PIC INT1M**	IM17	IM16	IM15	IM14	IM13	IM12	IM11	IM10
-0200H	**PIC INTR**	IR7	IR6	IR5	IR4	IR3	IR2	IR1	IR0
-0300H	**PIC INTEN**	0	0	0	0	TOV EN	0	INT EN	NMI EN

The INT0M and INT1M registers are used to mask interrupts input to INT0 and INT1, respectively. When bits IM0x and IM1x are 1, the corresponding interrupts are enabled. If more than one bit is selected, the interrupt is made active by ORing these bits.

The INTR register indicates the status of the interrupts. When an interrupt is requested, the corresponding bit in the register is read as 1. This is not related to the state of the mask. An edge interrupt request is cleared by writing 1 to the corresponding bit in this register.

The following table lists the interrupt sources assigned to bits IM0[0..7], IM1[0..7], and IR[0..7].

IM0,IM1,IR	Interrupt source	Request level
0	Timer 0 (mode 2)	Edge (rising)
1	Serial 0	Level (low)
2	Host (PCI communication)	Level (low)
3	Time-out	Level (low)
4	Timer 1 (mode 2)	Edge (rising)
5	Serial 1	Level (low)
6	Parallel (printer)	Level (low)
7	Not used (fixed to 0)	-

The INTEN register is used to enable and disable each interrupt type.

NMIEN: Specifies whether to mask a nonmaskable interrupt (NMI). Masking with this bit disables the NMI by means of hardware. At this point, the NMI pin is held high.

NMIEN	NMI	
0	To be masked	(Reset value)
1	To be used	

INTEN: Specifies whether to mask external interrupts (INT0 to INT3) used on the evaluation board. Masking with this bit disables INT0 to INT3 by means of hardware. At this point, the INTx pin is held high.

INTEN	INT0 to INT5	
0	To be masked	(Reset value)
1	To be used	

TOVEN: Specifies whether to use the time-out function. This function is used for accessing the local bus. If the bus cycle lasts for about 8 μs, the bus cycle is forcibly terminated.

TOVEN	Time-out
0	To be masked (Reset value)
1	To be used

5.4.7. PCI Controller

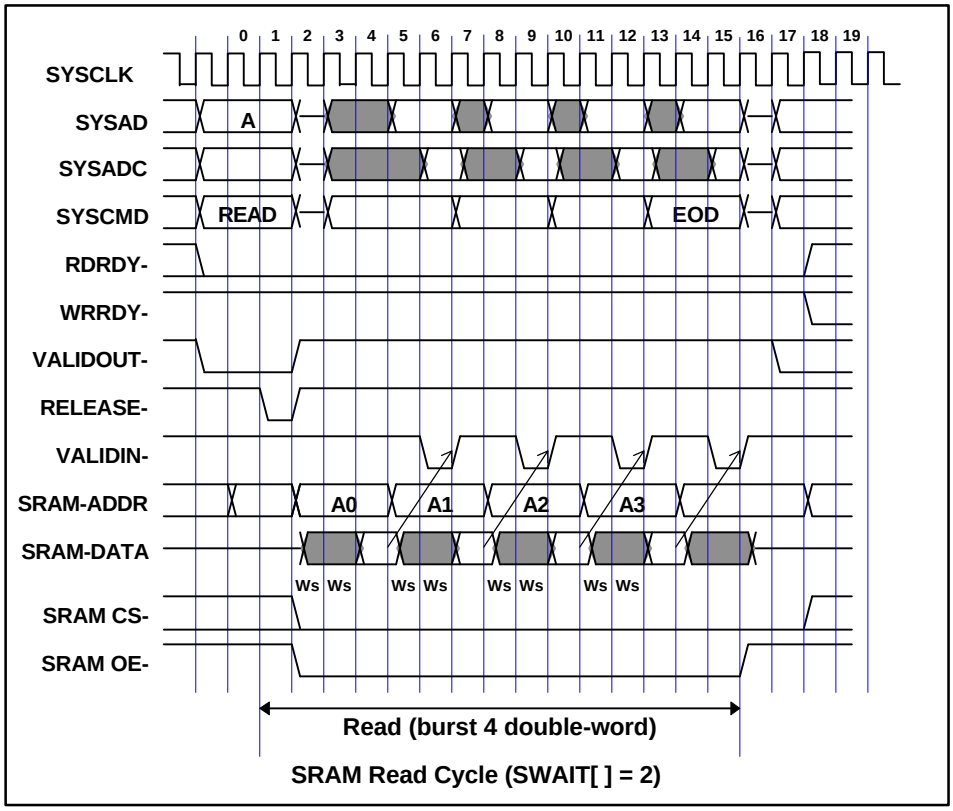
PLX Technology' s PCI9060ES is used for PCI bus communication. Because the PCI9060ES uses an endian control pin, its internal registers support both big and little endian modes.

5.5. BUS CYCLE TIMING

The RTE-VR5000-PC controls the bus cycles for the devices such as SRAM, DRAM, ROM, and I/O. This section describes the timing of each access cycle.

5.5.1. SRAM Access

0 to 3 wait states are inserted into the SRAM read cycle according to the setting of the SRAM-SWAIT register. (See Section 5.4.1.) No-wait access is possible only when the frequency of the bus clock (SYSCLK) is 40 MHz or less.



SRAM Read Cycle (SWAIT[ ] = 2)

The following paragraphs explain the above timing chart according to the clock cycle number.

0: Usually, RDRDY is active, while WRRDY is inactive.

1: The external read cycle of the CPU begins.

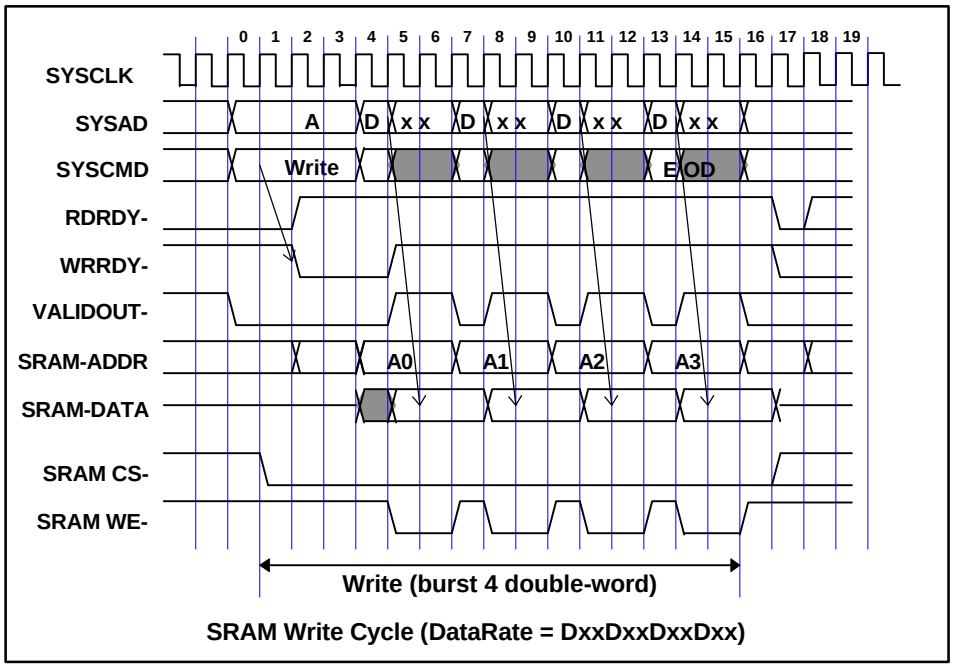
2 and 3: A specified number of wait states are inserted (in this example, two wait states are specified in SWAIT).

4: Data in SRAM is asserted. The SRAM address will be changed during the next cycle (subaddress).

5 and 6: Data is latched, and VALIDIN will be returned after two clock cycles. During this two-clock cycle, the data parity for the SYSADC bus is calculated.

7 to 15: The access cycle is repeated until the final data (EOD) is reached.

The SRAM write cycle follows the output data rate of the CPU. The SRAM cycle is started by returning WRRDY 1 clock cycle after the address is asserted.



SRAM Write Cycle (DataRate = DxxDxxDxxDxx)

The following paragraphs explain the above timing chart according to the clock cycle number.

0: Usually, RDRDY is active, while WRRDY is inactive.

1: The SRAM write cycle is asserted.

2: WRRDY is activated, and RDRDY is deactivated. The external write cycle of the CPU will begin after two clock cycles.

4: The first output data is now available. It is latched, and, during the next cycle, WRRDY is deactivated while SRAM WE is activated.

5 and 6: This is the SRAM write cycle. (In this example, the write pulse width is 2 clock cycles, because the data rate is Dxx. For the Dx pattern, the write pulse width is 1 clock cycle. For the Dxxx pattern, the write pulse width is 3 clock cycles.) Before the next data is latched, WE- is deactivated, and the SRAM address will be changed on the next cycle (sequential address).

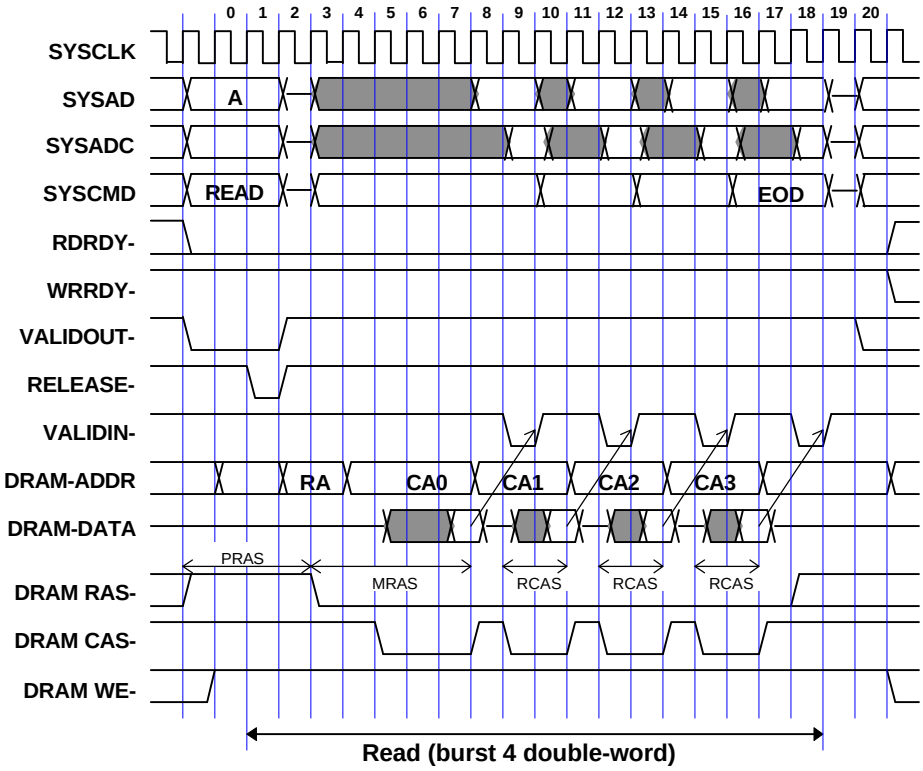
7 to 15: The write cycle is repeated.

16: RDRDY is activated during the first cycle after the last data (EOD) is written.

5.5.2. DRAM Access

For DRAM, the RAS/CAS width can be controlled according to the setting of the DRAM controller. (See Section 5.4.2.)

The following is the timing chart of the DRAM read cycle (FPM-DRAM) when EDOEN = 0. Note that, in this example, the DRAM read cycle does not coincide with a fresh cycle or the RAS precharge cycle of the previous DRAM access cycle. Therefore, this is the fastest cycle.



DRAM Read Cycle (RCAS[ ] = 1, MRAS[ ] = 4, PRAS[ ] = 3, EDOEN = 0)

The following paragraphs explain the above timing chart according to the clock cycle number.

0: Usually, RDRDY is active, while WRRDY is inactive.

1: The DRAM read cycle begins.

2 and 3: As the row address is asserted, RAS is activated.

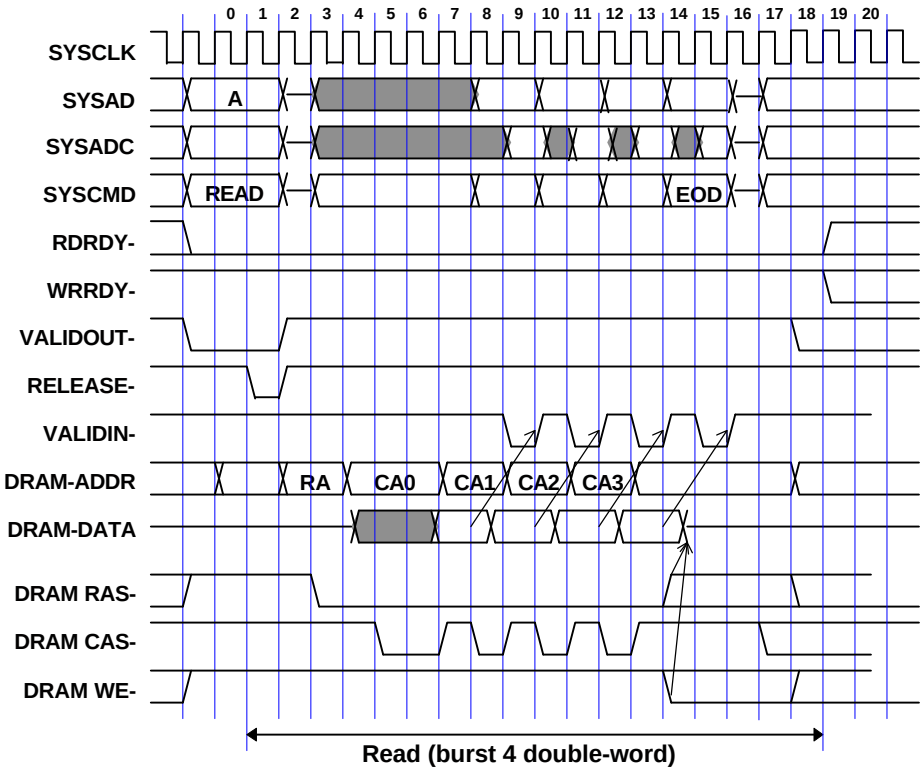
4 and 5: The column address is selected, and CAS is activated 2 clock cycles after RAS is activated.

7: The first read data is asserted. CAS is held until a cycle of DRAMC-MRAS+1.

8 and 9: Data is latched, and VALIDIN- will be returned after two clock cycles. During this two-clock cycle, the data parity for the SYSADC bus is calculated.

10 to 18: The access cycle is repeated until the last data (EOD) is reached. If HITEN = 1, RAS is held active.

If EDOEN = 1, the assertion of the read data is deferred 1 clock cycle to wait for the CAS precharge cycle. In this case, it may be possible to reduce the DRAMC-MRAS and DRAMC-RCAS values by one, depending on the SYSCLK width. In EDO-DRAM, data output is turned off by the WE- signal in the last cycle in order to hold the data until RAS becomes inactive.



DRAM Read Cycle (RCAS[ ] = 0, MRAS[ ] = 3, PRAS[ ] = 3, EDOEN = 1)

The following paragraphs explain the above timing chart according to the clock cycle number.

0: Usually, RDRDY is active, while WRRDY is inactive.

1: The DRAM read cycle begins.

2 and 3: As the row address is asserted, RAS is activated.

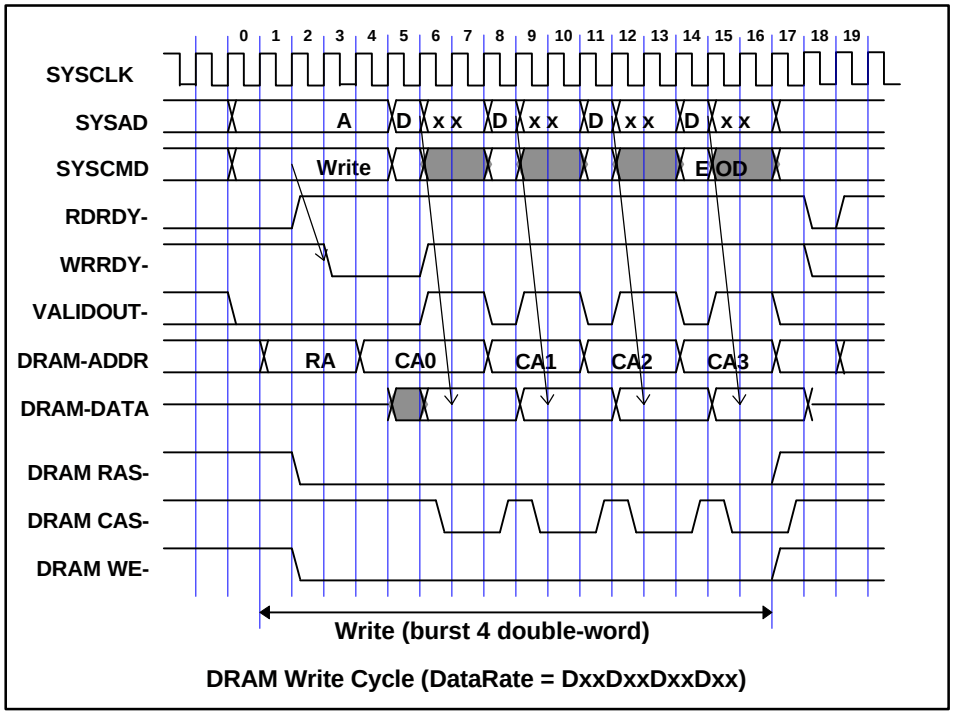
4 and 5: The column address is selected, and CAS is activated 2 clock cycles after RAS is activated.

6 and 7: The first read data is asserted. CAS is held until a cycle of DRAMC-MRAS+1.

8 and 9: Data is latched, and VALIDIN will be returned after two clock cycles. During this two-clock cycle time, the data parity for the SYSADC bus is calculated.

10 to 15: The access cycle is repeated until the last data (EOD) is reached. If HITEN = 1 at 14, RAS is held active, and data is placed in a high-impedance state by activating WE-.

The DRAM write cycle follows the output data rate of the CPU. The DRAM cycle is started by returning WRRDY 1 clock cycle after RAS becomes active. An early write cycle is used in DRAM write access.



DRAM Write Cycle (DataRate = DxxDxxDxxDxx)

The following paragraphs explain the above timing chart according to the clock cycle number.

0: Usually, RDRDY is active, while WRRDY is inactive.

1 and 2: The DRAM write cycle is asserted, and the row address and RAS become active. Because this is the write cycle, RDRDY is deactivated.

3 and 4: WRRDY is activated 1 clock cycle after RAS becomes active, and the external write cycle of the CPU begins 2 clock cycles after WRRDY is activated.

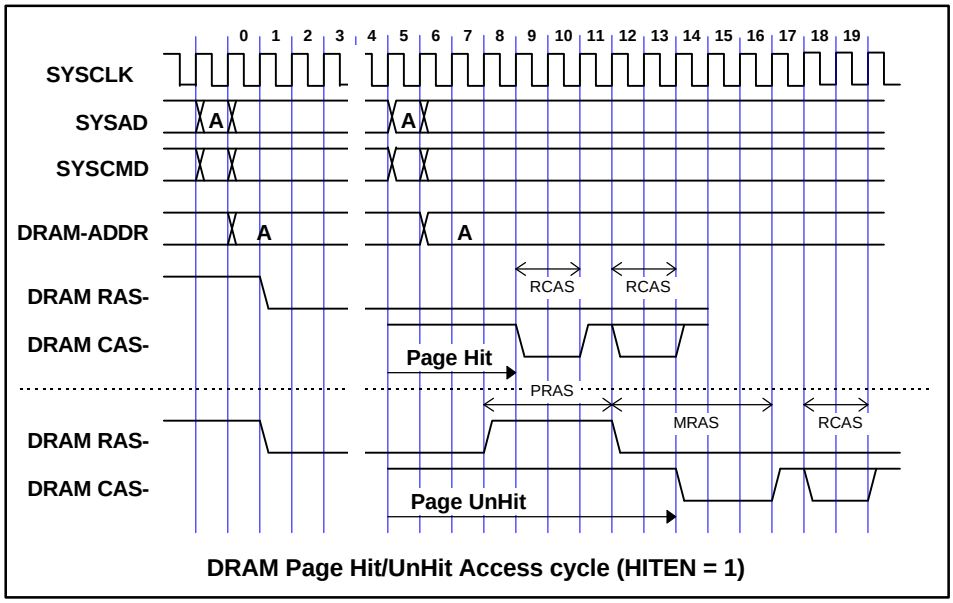
5: The first output data is now available. It is latched, and, during the next cycle, WRRDY will be deactivated.

7 and 8: This is the DRAM CAS write cycle. (In this example, the CAS write pulse width is 2 clock cycles, because the data rate is Dxx. For the Dx pattern, the CAS write pulse width is 1 clock cycle. For the Dxxx pattern, the CAS write pulse width is 3 clock cycles.) Before the next data is latched, WE is deactivated, and the DRAM address will be changed during the next cycle (sequential address).

9 to 16: The write cycle is repeated. RAS and WE are deactivated 2 clock cycles after the last data is written at 15. If HITEN = 1, RAS is held active.

17: RDRDY is activated during the first cycle after the last data (EOD) is written.

If HITEN = 1, the number of access cycles is reduced if the RAS held after DRAM access matches the row address for the next access (hit), because the CAS cycle is executed immediately. This takes effect only in the read cycle, however. In the write cycle, address comparison delays WRRDY by 1 clock cycle. If no match occurs (mishit), the overhead increases, because the RAS precharge precedes the usual RAS/CAS cycle access.



DRAM Page Hit/UnHit Access cycle (HITEN = 1)

The following paragraphs explain the above timing chart according to the clock cycle number.

0 to 4: This is the usual DRAM access cycle.

5: The next DRAM read access begins.

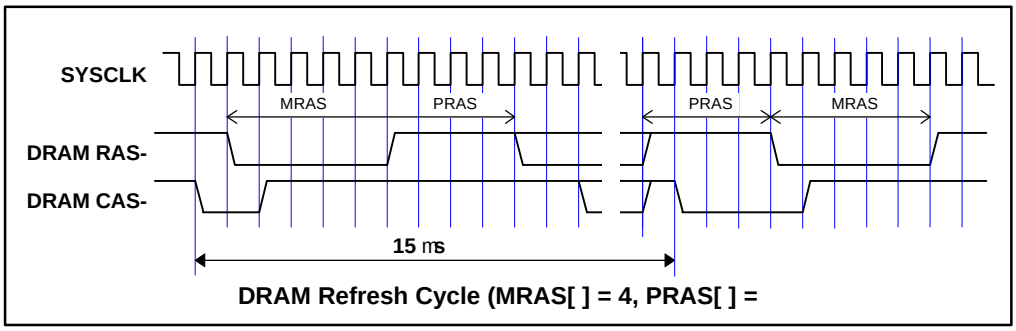
6: The row address is compared with the previous one.

7 to 8: If a match is detected, the read CAS will be activated during the next cycle. If no match is detected, RAS will be deactivated to trigger the RAS precharge.

9: The first CAS read cycle caused due to a match begins as page-mode access.

14: For the read CAS caused as a result of a mismatch, the usual RAS access cycle takes place.

The DRAM is refreshed using the CAS-before-RAS cycle at about 15 μs intervals (as specified in timer 2).

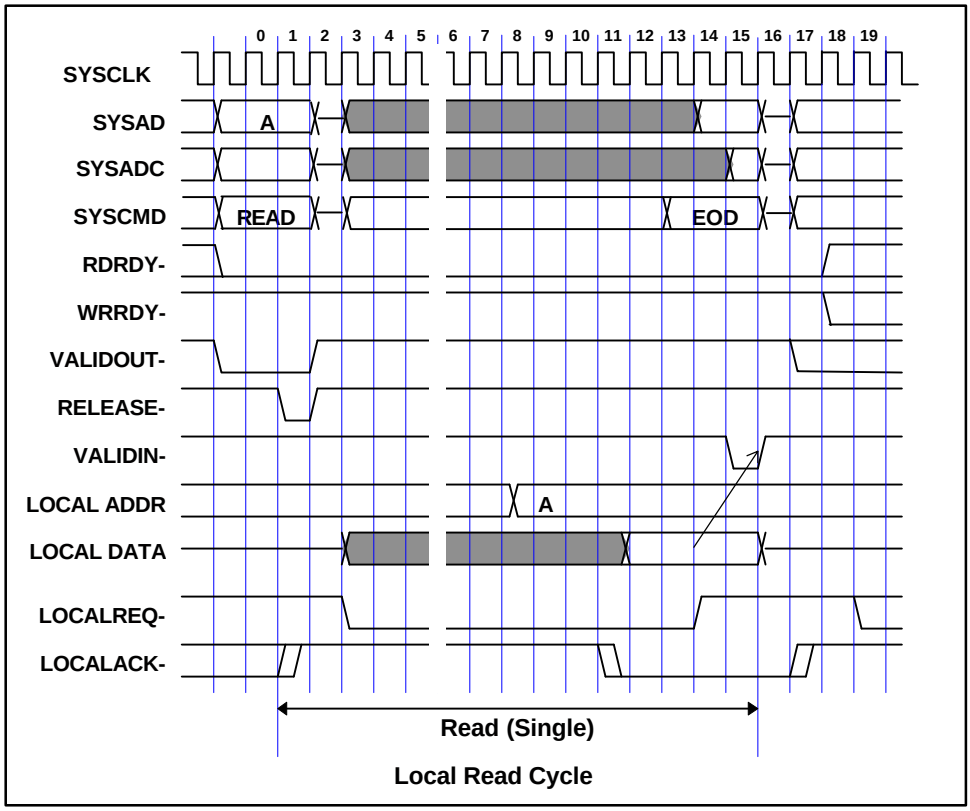


DRAM Refresh Cycle (MRAS[ ] = 4, PRAS[ ] =

5.5.3. Local Bus Access

The local bus has a data width of 16 bits. Its cycles are generated by the local bus controller according to a clock (with a fixed frequency of 32 MHz) that is asynchronous with the CPU clock. Only single-cycle access is allowed for the local bus. (Any attempt to perform burst-cycle read access results in a bus error, while any attempt to perform burst-cycle write access is ignored.) For single-cycle access, the control circuit in the CPU issues a request to the local bus controller, and performs arbitration based on the acknowledgment returned from the controller.

In the local bus read cycle, a read request is issued to the local bus controller and, after data is read, the controller returns acknowledgment.



The following paragraphs explain the above timing chart according to the clock cycle number.

0 to 3: Access to the local bus begins.

4 and after: After it has been confirmed that acknowledgment (LOCAKACK) is inactive, an access request (LOCALREQ) is issued to the local bus.

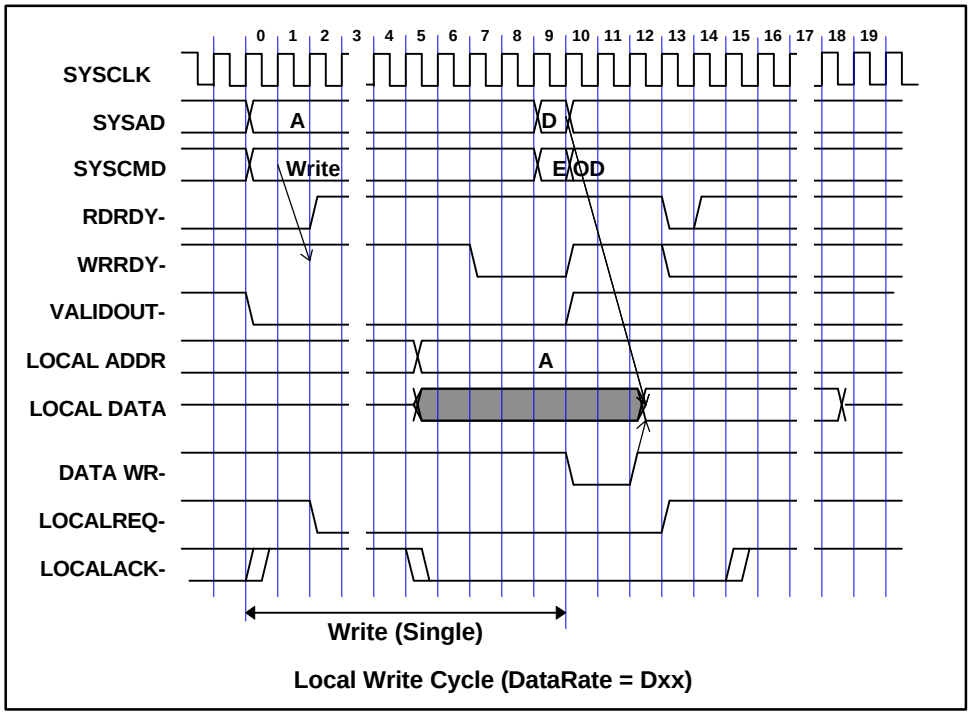
8: Upon detecting an access request, the local bus controller latches the address and begins the read cycle.

11: Upon the completion of the read operation, the local bus returns an acknowledgment.

13: The request is reset once acknowledgment has lasted for 2 clock cycles. VALIDIN is returned 2 clock cycles after the read data has been latched.

17: Upon detecting that the request has been reset, the local bus controller deactivates acknowledgment.

Similarly to the read access of the local bus, local bus write access is performed by request/acknowledgment arbitration. In this case, however, acknowledgment returned from the local bus controller is regarded as permission to write. Data writing is carried out in the acknowledgment cycle after the request is reset. During the data write cycle, the CPU can perform the next cycle except for the local bus.



Local Write Cycle (DataRate = Dxx)

The following paragraphs explain the above timing chart according to the clock cycle number.

0 and 1: Write access to the local bus begins.

2: After it has been confirmed that acknowledgment (LOCAKACK) is inactive, an access request (LOCALREQ) is issued to the local bus.

5: Upon detecting the access request, the local bus controller latches the address and returns acknowledgment.

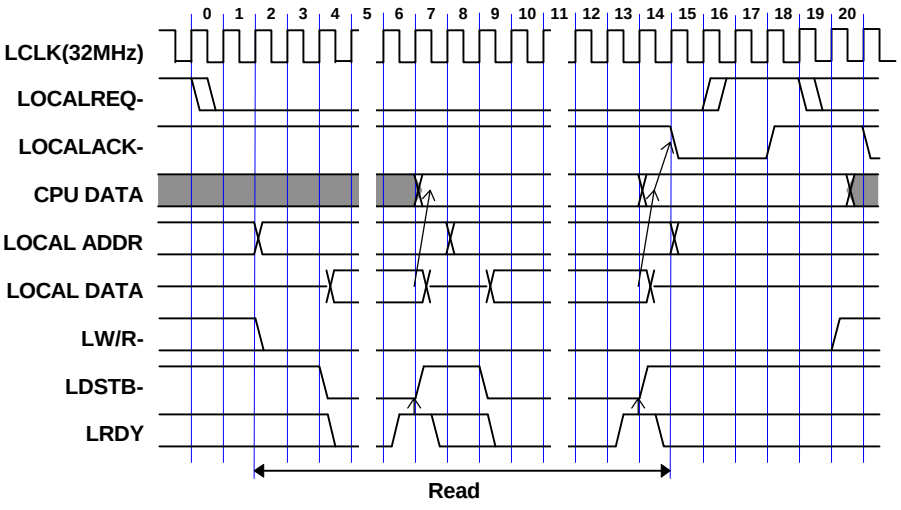
7: After the acknowledgment has lasted for 2 clock cycles, WRRDY is activated to cause the CPU to start a write cycle.

12 and 13: After write data has been sent on to the local bus, the write request is deactivated.

14 and 15: Upon detecting that the request has been reset, the local bus controller deactivates acknowledgment, then performs data writing.

The local bus controller accesses the local bus when the CPU requests single-cycle access. Because the CPU supports an access data width of up to 64 bits, while that of the local bus is 16 bits, up to 4 bus cycles can be generated by bus sizing.

The timing of the read cycle is as shown below:



Local-BUS Read Cycle

The following paragraphs explain the above timing chart according to the clock cycle number.

0 and 1: The read request to the local bus begins.

2: The local bus controller latches the address and read status (LW/R-).

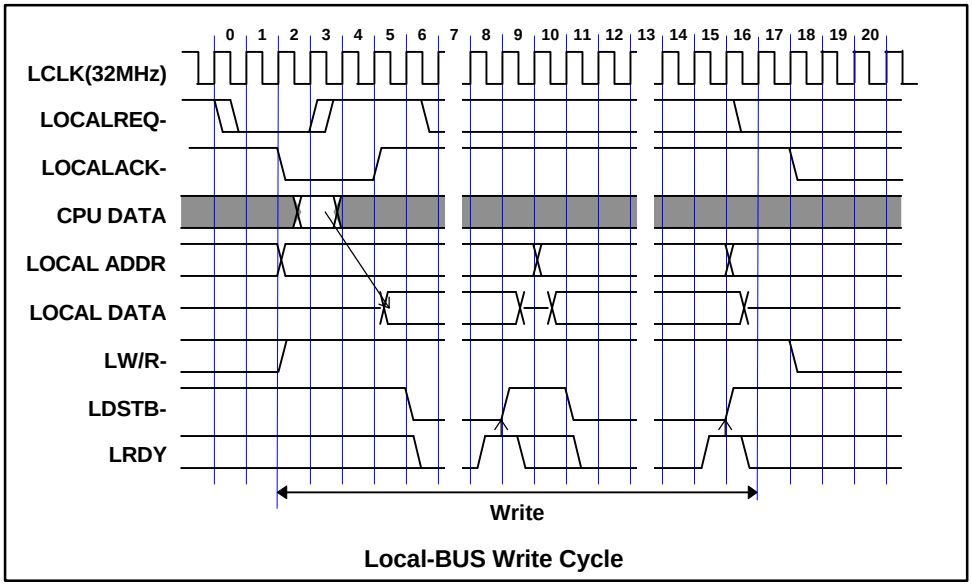
4: The data strobe (LDSTB) is activated to begin read access 2 clock cycles after the address is latched.

6 and 7: When the local bus ready signal (LRDY) is returned, the data strobe is deactivated to latch the CPU data.

8 to 14: If the data size of the CPU is larger than 16 bits, the next address is selected to repeat the read cycle.

15: Once all read cycles have been completed, and the CPU data is asserted, acknowledgment is returned.

The timing of the write cycle is as shown below:



Local-BUS Write Cycle

The following paragraphs explain the above timing chart according to the clock cycle number.

0 and 1: The write request to the local bus begins.

2: The local bus controller returns acknowledgment, and latches the address and write status (LW/R-).

3 to 5: The write data is asserted 2 clock cycles after the request is deactivated. During the next cycle, the data strobe (LDSTB) is activated to begin write access.

8 and 9: When the local bus ready signal (LRDY) is returned, the data strobe is deactivated to finish the write cycle.

10 to 15: If the data size of the CPU is larger than 16 bits, the next address is selected to repeat the write cycle.

17: Once all write cycles have been completed, another request is accepted.

The local bus ready signal (LRDY) differs from the address space assigned to the local bus as listed below:

Local bus address space	Ready signal Local bus clock at 32 MHz	Remark
ROM	5 LCLK (about 150 ns)	Fixed
I/O ***1**	7 LCLK (about 210 ns)	Fixed
EXT-BUS	ERDY (EXT-BUS ready)	
PCI controller	PCI controller ready signal	
No assignment ***2**	Time-out ready (about 8 μs)	Fixed

***1** The local bus controller supports an I/O access inhibit period of 7 clock cycles (about 210 ns) after I/O access for some hardware, because the I/O device has a fixed inactive period for the RD/WR signal in continuous access. This eliminates the necessity for the software to insert wait states after an I/O access cycle.

***2** When the time-out function is available (see Section 5.4.6).

5.5.4. Memory Controller Register Access

Only single-cycle access is allowed for the SRAM and DRAM memory controller registers. (Any attempt to perform burst-cycle read access results in an error, while any attempt to perform burst-cycle write access is ignored.) The timing of access to this address space is similar to that of SRAM access with one wait state. (See Section 5.5.1.)

5.5.5. Secondary Cache Access

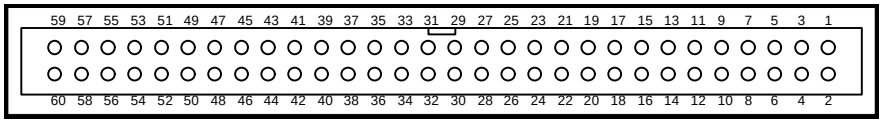
For an explanation of the access timing of an optional secondary cache board, refer to the applicable processor manual. External read access begins after a cache mishit (when the cache and external memory are not accessed simultaneously). Flashing in page units is not supported for cache instructions usable for the secondary cache, so flashing should be performed for all of memory or by using the TAG store.

5.6. EXT-BUS SPECIFICATION

The EXT-BUS is used to expand memory and I/O units. The local bus on this board is connected to the JEXT connector.

5.6.1. JEXT Connector

The shape and pin arrangement of the JEXT connector are shown below:



JEXT Connector Pin Arrangement

Number	Signal name	Number	Signal name	Number	Signal name	Number	Signal name
1	**+5 V**	2	**+5 V**	31	**GND**	32	**GND**
3	D0	4	D1	33	A8	34	A9
5	D2	6	D3	35	A10	36	A11
7	D4	8	D5	37	A12	38	A13
9	D6	10	D7	39	A14	40	A15
11	**GND**	12	**GND**	41	**+5 V**	42	**+5 V**
13	D8	14	D9	43	A16	44	A17
15	D10	16	D11	45	A18	46	A19
17	D12	18	D13	47	BHE-	48	**GND**
19	D14	20	D15	49	**GND**	50	RD-
21	**+5 V**	22	**+5 V**	51	WR-	52	RESET-
23	A0	24	A1	53	**GND**	54	**GND**
25	A2	26	A3	55	READY	56	INT-
27	A4	28	A5	57	**GND**	58	**GND**
29	A6	30	A7	59	LBCLK	60	**GND**

JEXT Connector Signal Name

Signal name	Input/ output	Function	Remarks
+5 V	-	Supply voltage of +5 V	
GND	-	Ground	
A[1..19]	Output	Address bus signal	
A0	Output	Byte low enable signal, which is active when bits D[0..7] are enabled	
BHE-	Output	Byte high enable signal, which is active when bits D[8..15] are enabled	
D[0..15]	Input/ output	Data bus signal, which buffers the CPU data bus	
RD-	Output	Read cycle timing signal, which becomes active only when the EXT-BUS space is accessed	
WR-	Output	Write cycle timing signal, which becomes active only when the EXT-BUS space is accessed	
READY	Input	Positive logical ready signal indicating the end of a cycle. It is valid only for the EXT-BUS space. It is pulled up with a 1 kΩ resistor on the board.	*1
INT-	Input	Active-low interrupt request signal, which is connected to the INT2- pin of the CPU via a buffer. It is pulled up with a 1 kΩ resistor on the board.	
RESET-	Output	Active-low system reset signal	
LCLK	Output	Bus clock signal (fixed to 32 MHz)	*2

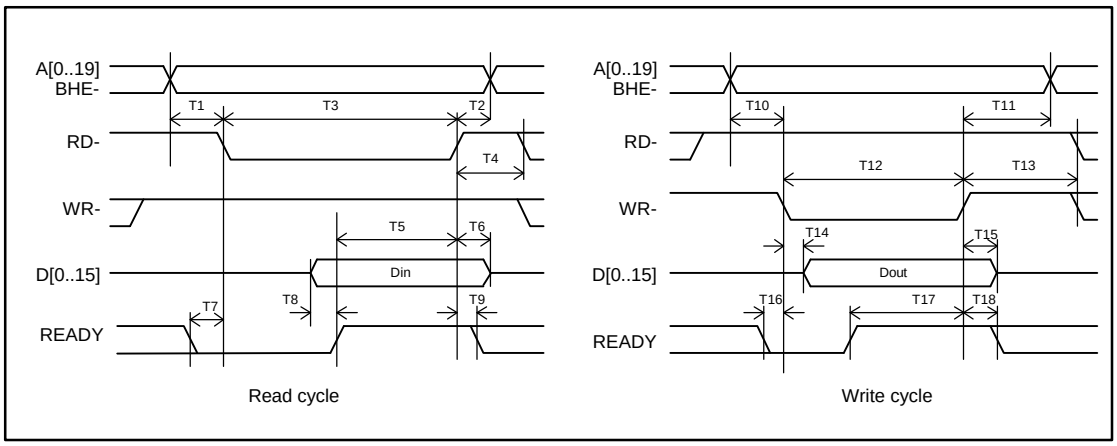
EXT-BUS Signals

*1 To have the CPU recognize READY securely, it is necessary to keep READY active until RD- or WR- becomes inactive.

*2 This clock signal differs from that used on other RTE series evaluation boards. It should not be used if the design is intended for general use.

5.6.2. EXT-BUS Timing

The EXT-BUS timing is shown below:



EXT-BUS Cycle

Symbol	Description	MIN (ns)	MAX (ns)
T1	RD address setup time	0	
T2	RD address hold-up time	0	
T3	RD cycle time	50	
T4	RD cycle interval	20	
T5	RD data setup time	15	
T6	RD data hold time	0	
T7	RD READY WAIT setup time	0	
T8	RD READY setup time	0	
T9	RD READY hold time	0	
T10	WR address setup time	0	
T11	WR address hold time	20	
T12	WR cycle time	50	
T13	WR cycle interval	20	
T14	WR data delay time	0	20
T15	WR data hold time	20	
T16	WR READY WAIT setup time	0	
T17	WR READY setup time	0	
T18	WR READY hold time	0	

EXT-BUS AC Specifications

5.6.3. Cautions Related to EXT-BUS

Use of the address/data bus varies with the VR5000 endian mode used, as shown below:

VR5000 ADDR/DATA

A + 0	D63-56	D55-48	D47-40	D39-32	D31-24	D23-16	D15-08	D08-00

EXT-BUS ADDR/DATA

BIG-ENDIAN

A19-A1	BHE-	A0
A + 0	D63-56	D55-48
A + 2	D47-40	D39-32
A + 4	D31-24	D23-16
A + 6	D15-08	D08-00

LITTLE-ENDIAN

A19-A1	BHE-	A0
A + 0	D15-08	D08-00
A + 2	D31-24	D23-16
A + 4	D47-40	D39-32
A + 6	D63-56	D55-48

6. MULTI MONITOR

The ROM chip on the board is incorporated with the MULTI monitor. The following cautions should be observed when the board is connected to the MULTI server as the host.

6.1. MONITOR WORK RAM

The monitor uses (reserves) the SRAM area between the start address and 10000H (64 KB) as work RAM. In other words, user programs are not allowed to use logical addresses 8000-0000H to 8000-FFFFH and A000-0000H to A000-FFFFH. This is also true for the image area of this area.

6.2. INTERRUPTS

When running on the MULTI motor, user programs cannot debug interrupts. The monitor uses the INT0 interrupt.

6.3. _INIT_SP SETTING

_INIT_SP (stack pointer initial value) is set to 8007-FFFCH (highest SRAM address) by the monitor. (_INIT_SP can be changed in the MULTI environment.)

7. RTE COMMANDS

When the monitor and MIDAS server (RTESERV) are connected with the MULTI debugger, the TARGET window is opened. The RTE commands can be issued in this window. The following table lists the RTE commands.

Command	Description
HELP, ?	Displays help messages.
INIT	Initializes.
VER	Displays the version number.
CACHEFLUSH	Flushes the cache.
SHOWTLB	Displays the contents of the TLB.
IOREAD	Reads I/O data (with a size specified).
IOWRITE	Writes I/O data (with a size specified).

RTE Commands

Some commands require parameters. All numeric parameters such as addresses and data are assumed to be hexadecimal numbers. The following numeric representations are invalid:

0x1234, 1234H, $1234

7.1. HELP (?)

<Format> HELP [command-name]

The HELP command displays a list of RTE commands and their formats. A question mark (?) can also be used in place of the character string HELP. If no command name is specified in the parameter part, the HELP command lists all usable commands.

<Example> HELP INIT

Displays help messages for the INIT command.

7.2. INIT

<Format> INIT

The INIT command initializes the RTE environment. Usually, this command should not be used.

7.3. VER

<Format> VER

The VER command displays the version number of the current RTE environment.

7.4. CACHEFLUSH

<Format> CACHEFLUSH

The CACHEFLUSH command flushes the contents of the cache in the CPU.

7.5. SHOWTLB

<Format> SHOWTLB

The SHOWTLB command lists the contents of the TLB in the CPU.

7.6. IOREAD

<Format> IOREAD [BYTE|SHORT|LONG] [address]

The IOREAD command reads memory at the specified address according to the specified size, and displays the data. Select BYTE, SHORT, or LONG to specify 8, 16, or 32 bits. Use this command to access memory mapped I/O.

<Example> IOREAD BYTE BC000100
BC000100: 1A

7.7. IOWRITE

<Format> IOWRITE [BYTE|SHORT|LONG] [data] [address]

The IOWRITE command writes the specified data to memory at the specified address according to the specified size. Select BYTE, SHORT, or LONG to specify 8, 16, or 32 bits. Use this command to access memory mapped I/O.

<Example> IOWRITE SHORT 30F0 BC00F000

8. ROM PROGRAMMING

This chapter provides information that should be referenced by the user who creates programs in ROM on this evaluation board.

8.1. INITIALIZATION

The reset processing routine sets the wait states necessary for the memory access controller after initializing the processor registers. To refresh DRAM, timer 2 is used for setting the refresh time.

```
<Processor' s internal initialization>
(The offset is 0 for little endian and 7 for big endian.)
[0xB8000000+offset].b <= 1          … 1 wait state for SRAM
[0xB8000400+offset].b <= 1          … 2 clock cycles as DRAM CAS width
[0xB8000500+offset].b <= 4          … 5 clock cycles for DRAM RAS access
[0xB8000600+offset].b <= 3          … 4 clock cycles for DRAM RAS precharge
[0xB8000700+offset].b <= 0          … EDO/HIT disable
[0xBC040300+offset].b <= 0xb4       … Timer 2 mode 2 (set to about 15 μs intervals)
[0xBC040200+offset].b <= 0x1f       … Lower count of timer 2
[0xBC040200+offset].b <= 0x00       … Higher count of timer 2
```

8.2. INTERRUPTS

It is necessary to enable the required interrupts by using the interrupt mask register once the peripheral I/O device has been initialized. It is also necessary to enable the INT/NMI.

Example of using timer interrupt 1:

```
<Processor interrupt disable>
(The offset is 0 for little endian and 7 for big endian.)
[0xBC040300+offset].b <= 0x74       … Time 1 mode 2 (set to about 10 ms intervals)
[0xBC040200+offset].b <= 0x20       … Lower count of timer 1
[0xBC040200+offset].b <= 0x4e       … Higher count of timer 1
[0xBC070100+offset].b <= 0x10       … INT1M timer 1 enable
[0xBC070200+offset].b <= 0x10       … INTR timer 1 interrupt clear
[0xBC070300+offset].b <= 0x02       … INT enable
<Processor interrupt enable>
```

[Memo] To use the NMI for controlling (breaking into) a ROM emulator, it is necessary to enable the NMI in the monitor program for the emulator.

8.3. ROM DATA ARRANGEMENT

When writing ROM data, it is necessary to observe the correspondence between the ROM address bank and the data bus. In the 272048 type (128K x 16 bits), banks are generated for every 64 Kbytes as standard with switches. If no bank is to be used, set 2 and 3 of SW3 to ON. See Sections 3.5 and 4.1 for details of the ROM banks.

When writing to ROM with a 16-bit data bus, the byte arrangement of the data may differ from the format of the ROM writer depending on the endian mode used. (For example, the program code may be in big endian mode, while the ROM writer supports little endian mode.) If this is the case, write data, using the ROM writer' s function for swapping the high-order 8 bits of the 16-bit data with the low-order 8 bits.

[Memo] When a ROM emulator is used, the monitor program for the emulator may not operate normally if the ROM banks are not disabled.

9. APPENDIX

9.1. JC1 AND JC2 CONNECTORS

JC1 pin	Signal name	JC1 pin	Signal name
A1	SYSADC4	B1	SYSADC5
A2	SYSAD32	B2	SYSAD33
A3	SYSAD34	B3	SYSAD35
A4	SYSAD36	B4	SYSAD37
A5	SYSAD38	B5	SYSAD39
A6	GND	B6	GND
A7	SYSAD40	B7	SYSAD41
A8	SYSAD42	B8	SYSAD43
A9	SYSAD44	B9	SYSAD45
A10	SYSAD46	B10	SYSAD47
A11	+3.3 V	B11	+3.3 V
A12	SYSADC6	B12	SYSADC7
A13	SYSAD48	B13	SYSAD49
A14	SYSAD50	B14	SYSAD51
A15	SYSAD52	B15	SYSAD53
A16	SYSAD54	B16	SYSAD55
A17	GND	B17	GND
A18	SYSAD56	B18	SYSAD57
A19	SYSAD58	B19	SYSAD59
A20	SYSAD60	B20	SYSAD61
A21	SYSAD62	B21	SYSAD63
A22	SCVALID	B22	SCMATCH
A23	GND	B23	GND
A24	SYSCLK	B24	SYSCLK
A25	GND	B25	GND
A26	/WRRDY	B26	/RDRDY
A27	/VALIDOUT	B27	/VALIDIN
A28	/EXTREQ	B28	/RELEASE
A29	+3.3 V	B29	+3.3 V
A30	/INT0	B30	/INT1
A31	/INT2	B31	/INT3
A32	/INT4	B32	/INT5
A33	/RESET	B33	/NMI
A34	GND	B34	GND
A35	/SCCWE0	B35	/SCCWE1
A36	/SCDCE0	B36	/SCDCE1
A37	/SCTCE	B37	/SCCLR
A38	/SCTDE	B38	(N.C)
A39	/SCTOE	B39	/SCDOE
A40	+5 V	B40	+5 V

JC1 Pin Arrangement

JC2 pin	Signal name	JC2 pin	Signal name
A1	(N.C)	B1	(SCENABLE)
A2	(SCSIZE0)	B2	(SCSIZE1)
A3	(N.C)	B3	(N.C)
A4	+3.3 V	B4	+3.3 V
A5	SYSCMD0	B5	SYSCMD1
A6	SYSCMD2	B6	SYSCMD3
A7	SYSCMD4	B7	SYSCMD5
A8	SYSCMD6	B8	SYSCMD7
A9	SYSCMD8	B9	SYSCMDP
A10	GND	B10	GND
A11	SYSADC0	B11	SYSADC1
A12	SYSAD0	B12	SYSAD1
A13	SYSAD2	B13	SYSAD3
A14	SYSAD4	B14	SYSAD5
A15	SYSAD6	B15	SYSAD7
A16	GND	B16	GND
A17	SYSAD8	B17	SYSAD9
A18	SYSAD10	B18	SYSAD11
A19	SYSAD12	B19	SYSAD13
A20	SYSAD14	B20	SYSAD15
A21	+3.3 V	B21	+3.3 V
A22	SYSADC2	B22	SYSADC3
A23	SYSAD16	B23	SYSAD17
A24	SYSAD18	B24	SYSAD19
A25	SYSAD20	B25	SYSAD21
A26	SYSAD22	B26	SYSAD23
A27	GND	B27	GND
A28	SYSAD24	B28	SYSAD25
A29	SYSAD26	B29	SYSAD27
A30	SYSAD28	B30	SYSAD29
A31	SYSAD30	B31	SYSAD31
A32	GND	B32	GND
A33	SCWORD0	B33	SCWORD1
A34	SCLINE0	B34	SCLINE1
A35	SCLINE2	B35	SCLINE3
A36	SCLINE4	B36	SCLINE5
A37	SCLINE6	B37	SCLINE7
A38	+3.3 V	B38	+3.3 V
A39	SCLINE8	B39	SCLINE9
A40	SCLINE10	B40	SCLINE11
A41	SCLINE12	B41	SCLINE13
A42	SCLINE14	B42	SCLINE15
A43	GND	B43	GND
A44	/COLDRESET	B44	VCCOK
A45	MODEIN	B45	MODECLK
A46	(N.C)	B46	ENDIAN
A47	JTDI	B47	JTDO
A48	JTMS	B48	JTCK
A49	(N.C)	B49	(N.C)
A50	+5 V	B50	+5 V

JC2 Pin Arrangement

- Memo -