RTE-1000-TP

Hardware User's Manual

RealTimeEvaluator

Notice

Trademarks

Revision History

Rev	Date(Y/M/D)	Contents
Rev.1.0	2000-3-6	Initial Revision

CONTENTS

1. OVERVIEW

RTE-1000-TP is an in-circuit emulator for NEC's RISC processor. By controlling the debugging control circuit (DCU) incorporated into the processor from the outside, RTE-1000-TP enables highly transparent emulation on the board.

The debugger may be Multi developed by GHS or PARTNER developed by MIDAS LAB.,INC, both of which operate under Windows 95/98/NT. The host system may be either a PC-9800 series or DOS/V machine.

The PC and RTE-1000-TP can be connected using a dedicated PCMCIA card, host card designed for a bus, LAN-BOX, etc., depending on the environment.

This product comes with the following components. First check that none of the components are missing.

1. RTE-1000-TP 1
2. User's manual 1
3. N-Wire cable 1
4. Power supply (RTE-PS03: +5V, 3.5A) 1

The following are required to use RTE-1000-TP, although they are not supplied with the product.

5. KIT-xxxx-TP <required.>

   This is the package depend on target processor, and includes followings.
   - RTE for Win32 Setup Disk
   - User's manual
   - License sheet

6. ROM emulator probes <Must be obtained as required.>

   Following probes and Adapters are available.
   - DIP-32-ROM Probe
   - Extend-STD-16BIT-ROM Probe
   - DIP-40-ROM Adapter: attached at the head of the Extend-STD-16BIT-ROM Probe
   - DIP-42-ROM Adapter: attached at the head of the Extend-STD-16BIT-ROM Probe

7. Host interface <One of the following is required.>

   One of the following is required:
   - PC card interface kit
   - PC 9800 Series DeskTop PC interface kit
   - DOS/V DeskTop PC ISA-bus interface kit
   - DOS/V DeskTop PC PCI-bus interface kit
   - LAN-BOX

8. Debugger <Either is required.>
   - GHS Multi
   - PARTNER/Win

2. MAIN FEATURES

High-level language debuggers

Both Multi and PARTNER are high-performance, high-level language debuggers that enable program execution, break point setting, variable inspection, and other operations to be performed at the source level.

Easy connection

RTE-1000-TP provides debugging capabilities equivalent to those of conventional in-circuit emulators, with the user system connected to the designated connector and the processor mounted on the board.

Highly transparent emulation

By controlling the debugging control circuit (DCU) incorporated into CPU from the outside, RTE-1000-TP provides highly transparent emulation, eliminating the problems associated with electrical interfaces.

ROM emulation

Up to 32Mbyte of ROM can be emulated. (shipped with 8Mbyte)

Probes and Adapters are available for expansion 16bit ROM connector, that supports DIP type ROM from 32 to 42 pin and emulation for on board ROM, such as flash ROM,

Real-time trace

RTE-1000-TP enables real-time trace, which is useful for debugging built-in systems. This capability uses a technique in which trace information conforming to the N-Wire specifications is recorded into memory, and supports trace clocks with frequencies of up to 66 MHz.

Communication with the host system via a dedicated card or LAN-BOX

Three types of cards and LAN-BOX are available.

- The PC card is of Type II, as defined in version 2.1 of the PCMCIA specifications (version 4.2 of the JEIDA specification), and is for note-type PCs.
- The host card is for desktop PCs equipped with the PC 9800 C bus or DOS/V ISA or DOS/V PCI bus.
- LAN-BOX is connected via a LAN, and is a 10Base-T interface.

3. HARDWARE SPECIFICATIONS

Emulation

Target device			NB85E, V831/2, VR5432, VR4122 (*1)
Emulation functions			
	Operating frequency		Depends on the CPU specifications(Refer to KIT-xxxx-TP)
	Interface		JTAG/N-Wire
*2	JTAG clk		100KHz - 25MHz
Break functions			
	H/W break points (execution addresses)		Depends on the CPU specifications(Refer to KIT-xxxx-TP)
	S/W break points		100
	Breaks that can be set using access events		Depends on the CPU specifications(Refer to KIT-xxxx-TP)
	Step breaks		Supported
	Manual breaks		Supported
	External breaks		Depends on the CPU specifications(Refer to KIT-xxxx-TP)
Trace functions			
	Trace data bus		4 bits
	Trace memory		4 bits x 128K words
	Trace delay		0 - 1FFFFh
*2	Trace clock		77 MHz (max.)
*2	Time tag		100us - 30h
	Trigger that can be set using an execution address		Depends on the CPU specifications(Refer to KIT-xxxx-TP)
*2	Trigger that can be set using an data access		Depends on the CPU specifications(Refer to KIT-xxxx-TP)
	Start that can be set using an execution address		Depends on the CPU specifications(Refer to KIT-xxxx-TP)
	Stop that can be set using an execution address		Depends on the CPU specifications(Refer to KIT-xxxx-TP)
	Data trace conditions		Depends on the CPU specifications(Refer to KIT-xxxx-TP)
	Disassembled trace data display function		Depends on the CPU specifications(Refer to KIT-xxxx-TP)
ROM emulation functions			
	Memory capacity		8M - 32 M-Byte
	Access time		40 ns(burst cycle:35nS) (*3)
	Operation Voltage		1.8V - 5V (*4)
	Electrical condition		LV-TTL(*5)
	Number of ROMs that can be emulated		
		DIP-32pin-ROM (8-bit ROM)	4 (max.)
		DIP-40/42pin-ROM (16-bit ROM)	2 (max.)
		Extend STD16BIT-ROM connector	2 (max.)
	Size of ROMs that can be emulated (bit)		
		DIP-32pin-ROM (8bits-bus)	1M, 2M, 4M, 8M (27C010/020/040/080)
		DIP-40pin-ROM (16bits-bus)	1M, 2M, 4M (27C1024/2048/4096)
		DIP-42pin-ROM (16bits-bus)	8M, 16M (27C8000/16000)
		Extend STD16BIT-ROM (16bits-bus)	1M, 2M, 4M, 8M, 16M, 32M, 64M, 128M, 256M
	Bus width specification (bits)		8/16/32
Pin mask functions			Depends on the CPU specifications(Refer to KIT-xxxx-TP)

*1: Including the products under development. RTE-1000-TP covers the both kits of RTE-100-TP and RTE-200-TP. It is planed to support new type of processors in turn, however, this does not imply any assurance to support all upcoming processors in the future.

*2: These are the items of enhancement from RTE-100/200-TP.

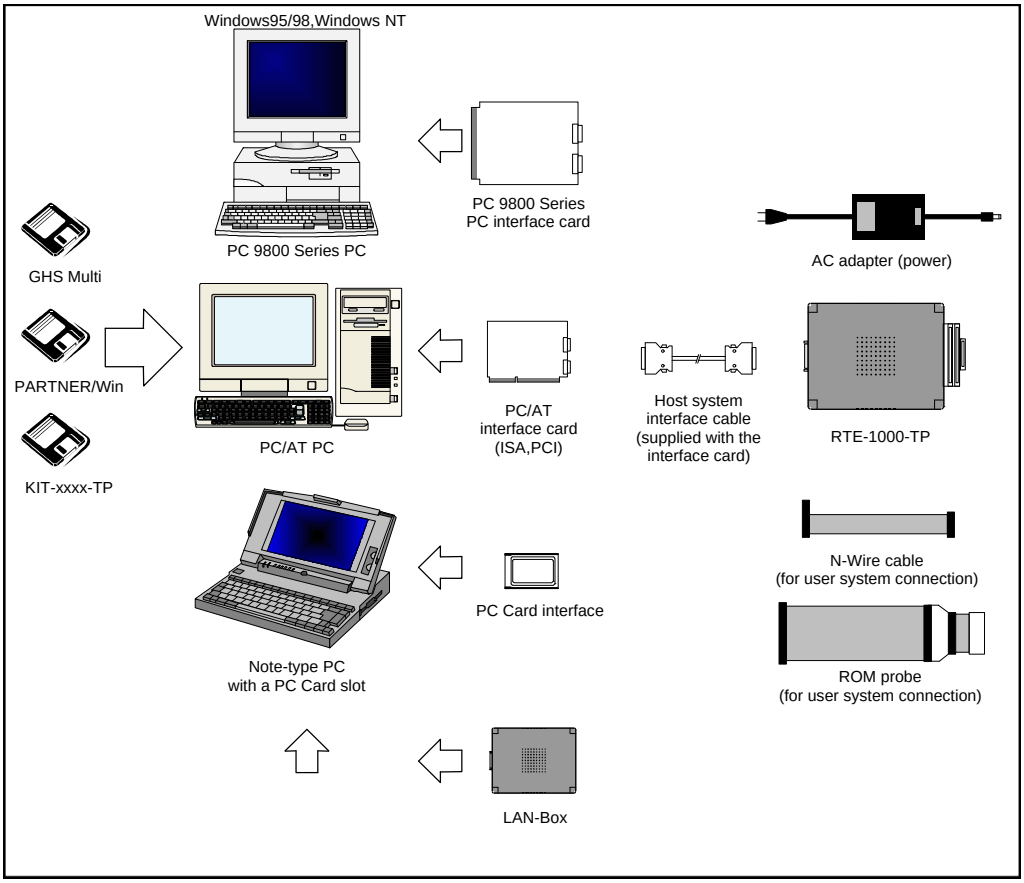
*3,4,5: These values are in the case that Extend-STD-16BIT-ROM Cable (CBL-STD16-32M) and DIP40/42 Adapter are used.

Host system and interface

Item	Description
Target host machine	PC 9800 Series and DOS/V PCs
Debugger	GHS-Multi , Partner/Win(Windows 95/98/NT)
Interface	PC card Type II (version 2.1 of the PCMCIA specifications/version 4.2 of the JEIDA specification or later) PC 9800 (C bus), PC/AT (ISA bus and PCI bus), or LAN-BOX
Power supply	AC adapter (in: 100 V out: +5 V, 2A)

4. SYSTEM CONFIGURATION

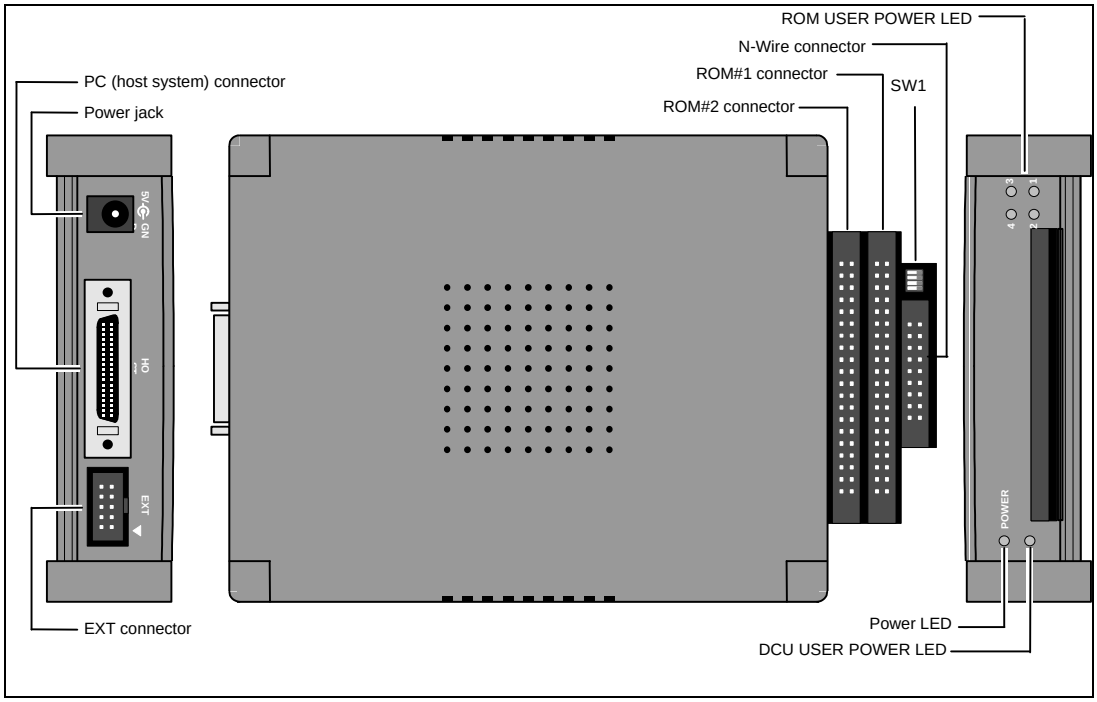
The following figure shows the configuration of a system in which RTE-1000-TP is used.



GHS-multi,PARTNER/Win:	High-level language debuggers for RTE-xxxx-TP
KIT-xxxx-TP	Control software for each processor
PC:	PC capable of running Windows 95
PC 9800 Series PC interface card:	Card supporting the PC 9800 C bus
PC/AT interface card:	Card supporting the PC/AT ISA bus or PCI bus
PC Card interface:	Type II card (version 2.1 of the PCMCIA specifications/ version 4.2 of the JEIDA specification or later)
LAN-Box	LAN supporting the PC(10base-T)
Host system interface cable:	Cable for connecting RTE-1000-TP to the host card
AC adapter:	Dedicated power supply
RTE-1000-TP:	Main Emulation BOX
N-Wire cable:	Cable for connecting to the user system used for debugging
ROM probe:	Probe for ROM emulation

5. COMPONENT NAMES AND FUNCTIONS

This chapter shows the appearance of RTE-1000-TP, as well as the names and functions of its components.



Power jack

This is a connector for the power supply. Power is supplied by inserting the plug of the supplied power supply into the jack.

> **Do not connect any device other than the supplied AC adapter (RTE-PS03) to the power jack.**

PC (host) connector (HOST)

This connector is used for connecting RTE-1000-TP to the PC (host system). The host system interface cable is connected to this connector.

EXT connector (EXT)

This connector is used for external signal input and internal signal output.

N-Wire connector (N-Wire connector: JDCU1)

This connector is used for connecting RTE-1000-TP to the user system via N-Wire.

ROM emulator connector #1 (ROM#1 connector: JROM1)

This is connector No. 1 for connecting RTE-1000-TP to the user system to emulate ROMs.

When the ROM emulated cable is used one, should use the ROM #1 connector.

ROM emulator connector #2 (ROM#2 connector: JROM2)

This is connector No. 2 for connecting RTE-1000-TP to the user system to emulate ROMs.

> **Cables of different types cannot be used to connect to JROM1 and JROM2. Be sure to use the cable of same type.**

Switch for setting mode (SW1)

This is the switch to set the mode of ICE itself. Usually set all to "OFF", unless otherwise specified.

Power LED (POWER)

This LED lights steadily while the power to RTE-1000-TP is on.

DCU user system power LED (DCU USER POWER LED: DCU POWER)

This LED lights steadily while the power to the user system connected with the N-Wire connector is on.

ROM user system power LEDs (ROM USER POWER LEDs: ROM POWER 1/2/3/4)

These LEDs light steadily while the power to the power pins of the ROM sockets connected with the ROM emulator connectors is on. The four LEDs have the following meanings:

If an 8-bit ROM probe is used:

LED1 to LED4 correspond to sockets ROM1 to ROM4 at the end of ROM probes, and light steadily when the power to the power pins of the sockets is on.

If a 16-bit ROM probe is used:

LED1 and LED2 light steadily at the same time while:

The power to ROM socket #1 connected with connector ROM#1 is on.

LED3 and LED4 light steadily at the same time while:

The power to ROM socket #2 connected with connector ROM#2 is on.

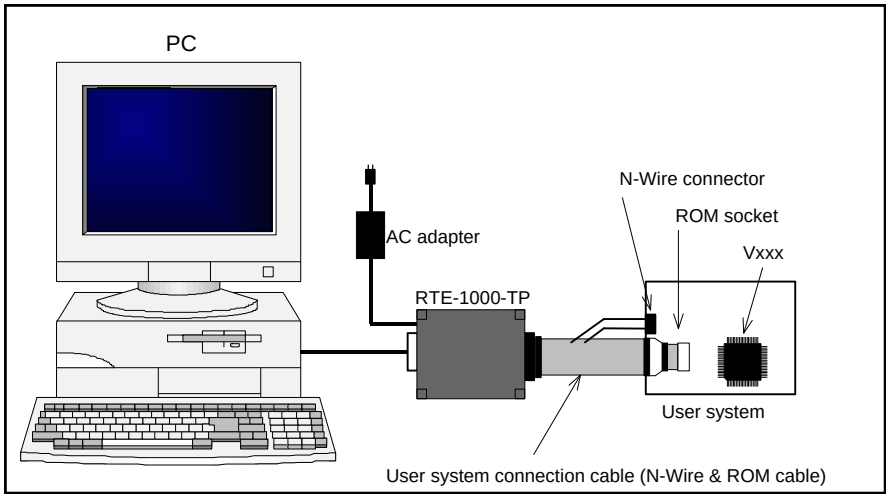
6. INSTALLATION PROCEDURE

This chapter describes the procedure for installing RTE-1000-TP.

1. **Mount the interface card.**
   Note For information, refer to the manual provided with the interface card.
2. **Install RTE for WIN32.**
   Note For information, refer to the manual provided with RTE for WIN32.

   At this point, do not start ChkRTE2.EXE.
3. **Connect RTE-1000-TP.**
   Connect RTE-1000-TP to the host interface card (or LAN-BOX) using the host system interface cable. Make the AC adapter ready for connection.
4. **Connect RTE-1000-TP to the user system.**
   Note For details, see Chapter 7.
5. **Turn on the power.**
   Note For details, see Chapter 8.
6. **Set RTE for WIN32.**
   Start ChkRTE2.EXE and set the necessary parameters. For details, refer to the manual provided with RTE for WIN32 or see Chapter 9 of this manual.
7. **Run the debugger.**
   Note For information, refer to the manual provided with the debugger.

The following figure shows an example how the devices are connected.



7. CONNECTION TO THE USER SYSTEM

The procedure for connecting RTE-1000-TP to the user system is described below.

Connection with the N-Wire cable

Connect the JDCU1 connector of RTE-1000-TP to the user system using the N-Wire cable supplied with RTE-1000-TP.

Connection with a ROM probe

Connect the JROM1 or JROM2 connector of RTE-1000-TP to the ROM socket of the user system, using a ROM probe of a type appropriate for the ROM of the user system. (ROM probes are options.)

Four types of ROM probe are available:

<DIP-32-ROM probe>

This probe allows emulation of up to four 8-bit ROMs.

On the RTE-1000-TP side, connect a probe labeled ROM1 and ROM2 to JROM1 and a probe labeled ROM3 and ROM4 to JROM2.

On the user system side, connect ROM1, ROM2, ROM3, and ROM4 to the ROM sockets with the lowest, second lowest, second highest, and highest addresses, respectively, if an 8-bit bus is used. If a 16-bit bus is used, connect ROM1/ROM2 to the ROM sockets corresponding to D0-D7/D8-D15 of the lower addresses and ROM3/ROM4 to the ROM sockets corresponding to D0-D7/D8-15 of the higher addresses.

<Extend-STD-16BIT-ROM Probe (Using DIP-40 and 42 Adapters is similar to this)>

These probes enable the emulation of up to two 16-bit ROMs.

Regarding the connection to user system using 16 bit bus, JROM1 and JROM2 are connected from the ROM socket of lower address respectively. In case of 32 bit bus, JROM1 is connected to the ROM socket corresponding to D0-15 and JROM2 to D16-31 respectively.

When connecting probes to ROM sockets, pay careful attention to the ROM orientation. The dot mark indicates pin 1.

Note on the DIP-32-ROM probe

For 32-pin ROMs of 1MB or greater, there are two possible pin assignment schemes. Set the jumper on the board for the ROM cable according to the ROM being used.

OE-:24-pin,A16:2-pin : 1-2 Jumpered (factory setting)

OE-:2pin,A16:24-pin : 2-3 Jumpered

8. POWERING ON AND OFF

The procedures for powering the system on and off are described below. Complete all the steps in the installation procedure (such as cable connection) before powering the system on.

Powering on

1. Turn on the power to the host system.
2. Turn on the power to RTE-1000-TP. (Connect the dedicated AC adapter to the power jack of RTE-1000-TP.)
3. Turn on the power to the user system.
4. Start the debugger.

Powering off

1. Quit the debugger.
2. Turn off the power to the user system.
3. Turn off the power to RTE-1000-TP. (Disconnect the AC adapter from RTE-1000-TP.)
4. Turn off the power to the host system.

Do not turn on the power to the user system before powering on RTE-1000-TP. Doing so may cause a malfunction.

9. INTERFACE SPECIFICATIONS

This chapter describes the standard specifications of the connectors used for control that are required for the user system. Detail is depend on the CPU. See Kit-xxx-TP's manual.

Pin arrangement table

Pin number	Signal name	Input/output (user side)	Treatment (user side)
A1	TRCCLK	Output	33-Ω series resistor (recommended)
A2	TRCDATA0	Output	33-Ω series resistor (recommended)
A3	TRCDATA1	Output	33-Ω series resistor (recommended)
A4	TRCDATA2	Output	33-Ω series resistor (recommended)
A5	TRCDATA3	Output	33-Ω series resistor (recommended)
A6	TRCEND	Output	33-Ω series resistor (recommended)
A7	DDI	Input	10-kΩ pull-up
A8	DCK	Input	10-kΩ pull-down
A9	DMS	Input	10-kΩ pull-down
A10	DDO	Output	33-Ω series resistor (recommended)
A11	DRST-	Input	10-kΩ pull-down
A12	Reserve	------	Depends on the CPU specifications(Refer to KIT-xxxx-TP)
A13	Reserve	------	Depends on the CPU specifications(Refer to KIT-xxxx-TP)

Pin number	Signal name	Input/output (user side)	Treatment (user side)
B1-B10	GND	------	Connection to the power GND
B11	Reserve	------	Depends on the CPU specifications(Refer to KIT-xxxx-TP)
B12	Reserve	------	Depends on the CPU specifications(Refer to KIT-xxxx-TP)
B13	VDD	------	Connect to the power supply for CPU external bus.

Connectors

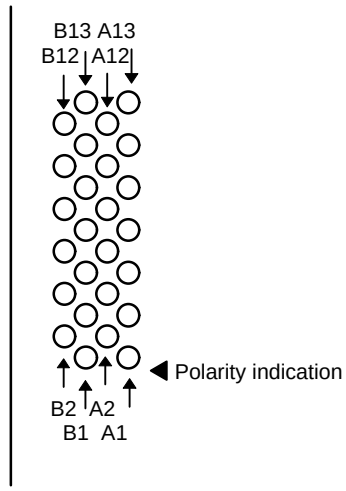
Manufacturer: KEL
Models: 8830E-026-170S (straight)
8830E-026-170L (right angle)
8831E-026-170L (right angle, fixing hardware attached)

Wiring and Wire Length

1.Keep the wire from CPU to the connector as short as possible.
>>100 mm or shorter is recommended.
2. Output signals from CPU are recommended to be connected to connectors, via high-speed CMOS buffers of which power supply is the same one with CPU I/O buffers.

Layout of the connectors on the board

The figure below shows the physical layout of the connectors on the board.



Board end [Top View]

Note: When actually arranging the pins, design them according to the connector dimensional information.

12. EXT CONNECTOR

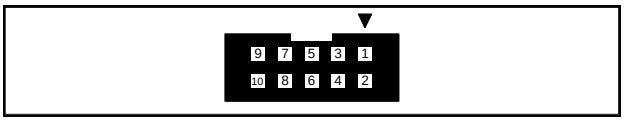
The specifications of the EXT connector are given below.

Pin number	Signal name	Input/output	Description
1	RSV-IN0	Output	Depends on the CPU specifications(Refer to KIT-xxxx-TP)
2	EXI0	Input	External input signal #0 (pulled up with a 1-kΩ resistor). Edge detectable.
3	RSV-IN1	Output	Depends on the CPU specifications(Refer to KIT-xxxx-TP)
4	EXI1	Input	External input signal #1 (pulled up with a 1-kΩ resistor)
5	RSV-OUT	Output	Depends on the CPU specifications(Refer to KIT-xxxx-TP)
6	EXI2	Input	External input signal #2 (pulled up with a 1-kΩ resistor)
7	RESETOUT-	Output	Output approximately 50mS of low level pulse by RESET command. (Open collector output, pull-up by 1K ohm)
8	EXI3	Input	External input signal #3 (pulled up with a 1-kΩ resistor)
9	GND	--	Ground signal
10	TRG-	Output	Trigger output that goes low upon detection of a trace trigger This signal is an open-collector signal (pulled up with a 1-kΩ resistor).

Notes:

1. The inputs to EXI0, EXI1, EXI2, and EXI3 are at LV-TTL level.
2. EXI0 can be specified as a trace trigger.
3. EXI0 to EXI3 are recorded in memory as trace information.
4. The pull-up resister is connected to the same voltage as JTAG-VCC.

Pin arrangement:



JEXT pin arrangement

Applicable connector:

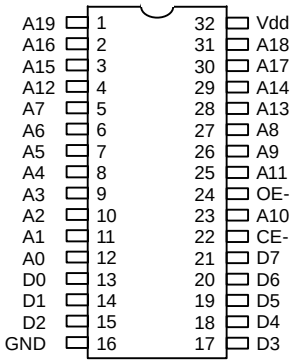
XG4M-1031 manufactured by Omron Corporation (or equivalent)

13. ROM PROBE SPECIFICATIONS

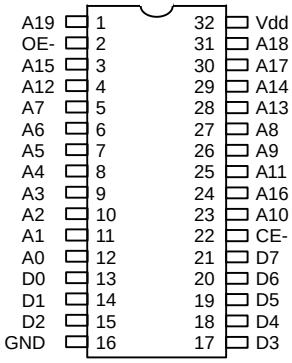
DIP-32-ROM probe

The DIP-32-ROM probe supports the following two pin arrangements. The arrangement to support is determined with the jumper on JP1.

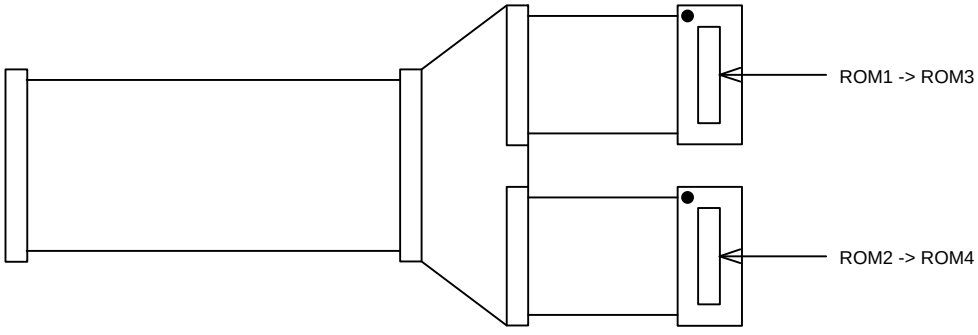
JP1 1-2 jumpered



JP1 2-3 jumpered

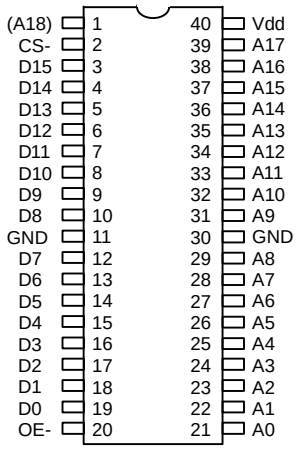


The labels at the end are marked ROM1 and ROM2 at the factory. If you purchase another DIP-32-ROM probe, replace the labels with those supplied to distinguish it from the first one, as shown in the figure below.



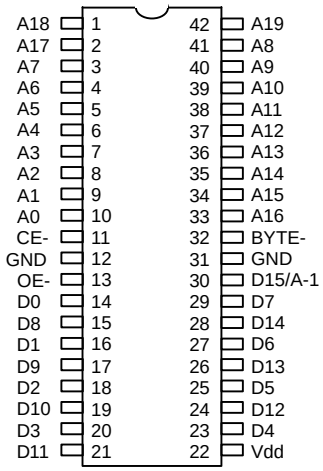
DIP-40-ROM adapter

The DIP-40-ROM adapter supports the following pin arrangement.



DIP-42-ROM adapter

The DIP-42-ROM adapter supports the following pin arrangement.



Extend-STD-16BIT-ROM probe

Signal description:

signal	IN/OUT	name	description
A0 - A23	IN	ADDRESS BUS	Connect to rom address. Not used address connect to gnd.
D0 - D15	OUT	DATA BUS	Connect to rom data
CE-	IN	CHIP ENABLE	ROM emulator is selected at LOW level.
OE-	IN	OUTPUT ENABLE	If CE- is LOW and this signal is LOW level, ROM emulator will drive the data bus.
WRL- WRH-	IN	Write low-byte Write High-byte	Connect the write signal of LOW active. This is not mandatory, but recommended for compatibility in the future.
PSENSE	IN	POWER SENSE	Connect to rom VDD
INH-	OUT	INHBIT-	ROM emulator always drives it to LOW level. Thus, this signal is pulled-up at target system side, so that it is possible to identify whether ROM emulator is connected. While ROM emulator is connected, be sure to disable the corresponding on board ROM at target system.
GND	-----	GND	Connect to ground.

Pin arrangement table:

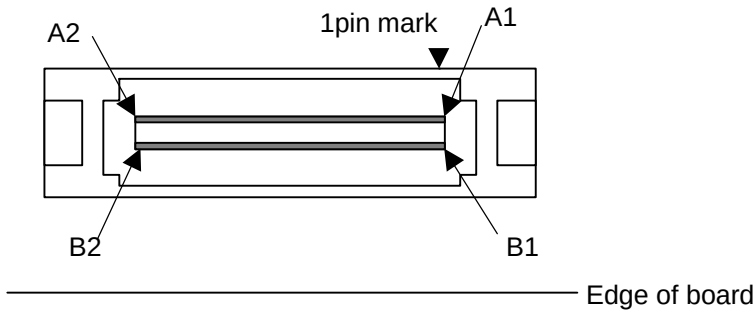
A side	signal	B side	signal
A1	GND	B1	A0
A2	A1	B2	A2
A3	A3	B3	A4
A4	A5	B4	A6
A5	A7	B5	A8
A6	A9	B6	A10
A7	A11	B7	A12
A8	A13	B8	A14
A9	A15	B9	A16
A10	A17	B10	A18
A11	A19	B11	A20
A12	A21	B12	A22
A13	NC.(WRH-)	B13	INH-(GND)
A14	NC.(WRL-)	B14	A23
A15	CE-	B15	GND
A16	OE-	B16	PSENSE(VCC IN)
A17	D0	B17	D1
A18	D2	B18	D3
A19	D4	B19	D5
A20	D6	B20	D7
A21	D8	B21	D9
A22	D10	B22	D11
A23	D12	B23	D13
A24	D14	B24	D15
A25	GND	B25	GND

Connectors:

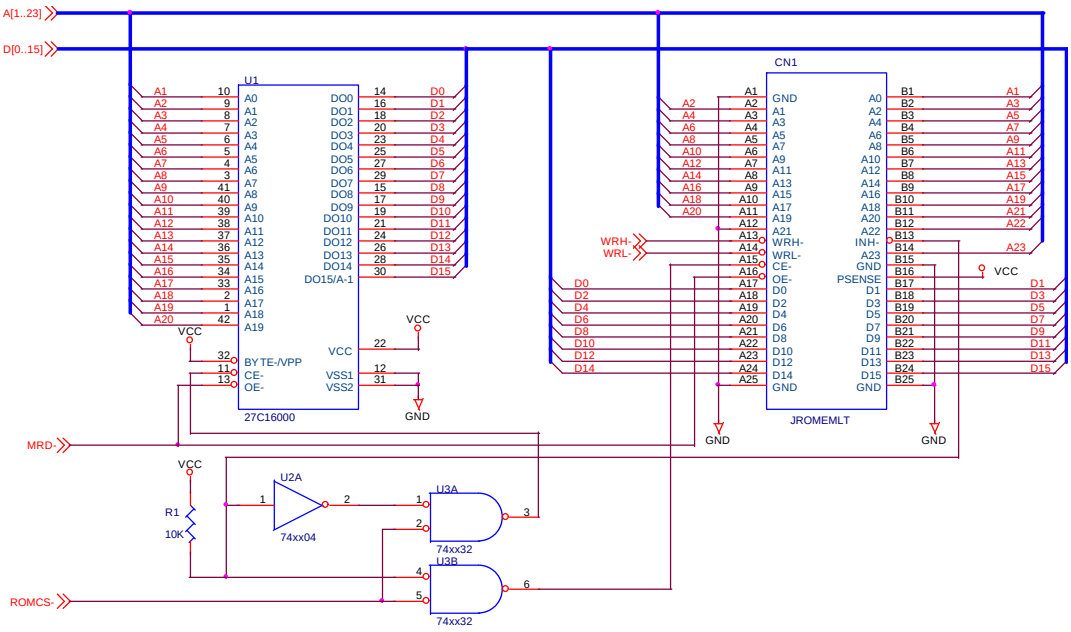
Manufacturer: KEL

Models: 8931E-050-178S (straight)
8931E-050-178L (right angle)
8930E-050-178MS(SMT straight)

Layout of the connectors on the board:

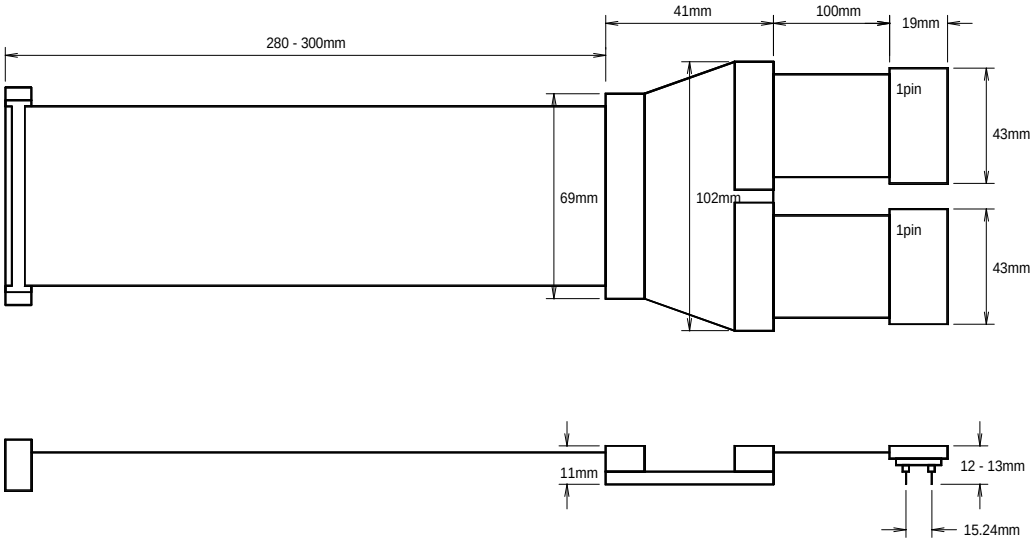


Reference of the schematic:

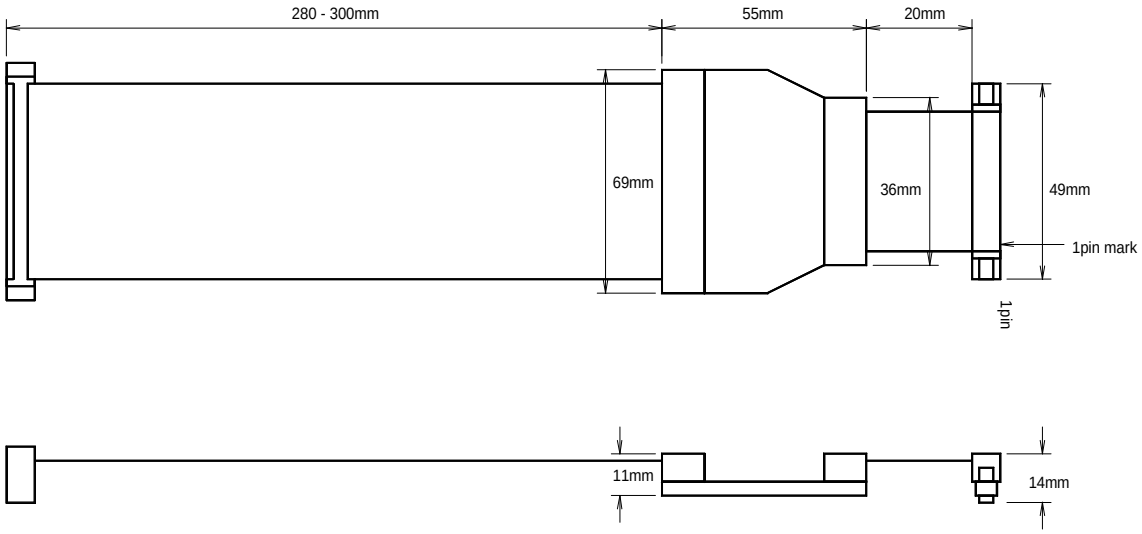


APPENDIX-A APPEARANCE of ROM PROBE

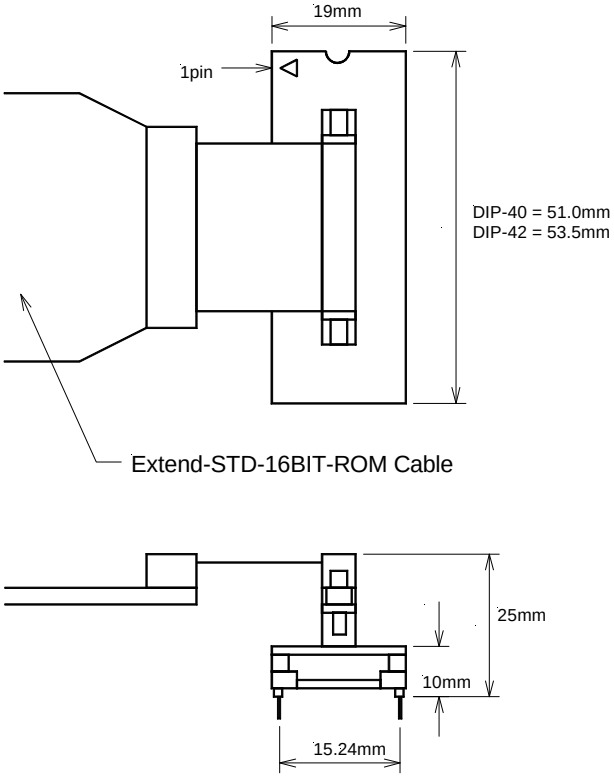
DIP-32-ROM probe



Extend-STD-16BIT-ROM probe



DIP-42-ROM adapter



APPENDIX-B Electrical Condition

JTAG/N-Wire Interface

DC Characteristics(2.7V < Vj <= 5.0V) :Vj=VDDjtag(B13)

Items		Symbol	Measurement Condition		Vj(V)	Min.	Max.	Unit
Input Voltage	"H" Level	VIH			2.7-5.0	1.6	5.5	V
	"L" Level	VIL			2.7-5.0		0.8	V
Output Voltage	"H" Level	VOH	VIN=VIH	IOH=-100uA	3.3-5.0	3.1		V
					2.7-3.3	Vj-0.2		
				IOH=-12mA	2.7	2.2		
				IOH=-18mA	3.0	2.4		
	"L" Level	VOL	VIN=VIL	IOL=30uA	2.7-5.0		0.2	
				IOL=12mA	2.7		0.4	
				IOL=18mA	3.0		0.4	

DC Characteristics(2.3V <= Vj <= 2.7V) :Vj=VDDjtag(B13)

Items		Symbol	Measurement Condition		Vj(V)	Min.	Max.	Unit
Input Voltage	"H" Level	VIH			2.3-2.7	1.6	5.5	V
	"L" Level	VIL			2.3-2.7		0.8	V
Output Voltage	"H" Level	VOH	VIN=VIH	IOH=-100uA	2.3-2.7	Vj-0.2		V
				IOH=-12mA	2.3	2.0		
				IOH=-18mA	2.3	1.8		
	"L" Level	VOL	VIN=VIL	IOL=40uA	2.3-2.7		0.2	
				IOL=12mA	2.3		0.4	
				IOL=18mA	2.3		0.6	

DC Characteristics(1.8V <= Vj < 2.3V) :Vj=VDDjtag(B13)

Items		Symbol	Measurement Condition		Vj(V)	Min.	Max.	Unit
Input Voltage	"H" Level	VIH			1.8-2.3	1.6	5.5	V
	"L" Level	VIL			1.8-2.3		0.8	V
Output Voltage	"H" Level	VOH	VIN=VIH	IOH=-100uA	1.8-2.3	Vj-0.2		V
				IOH=-6mA	1.8	1.4		
	"L" Level	VOL	VIN=VIL	IOL=60uA	1.8		0.2	
				IOL=6mA	1.8-2.3		0.3	

ROM Interface

DC Characteristics(2.7V < Vrom <= 5.0V) : Vrom is VDD pin voltage of ROM

Items		Symbol	Measurement Condition		Vrom(V)	Min.	Max.	Unit
Input Voltage	"H" Level	VIH			2.7-5.0	1.6	5.5	V
	"L" Level	VIL			2.7-5.0		0.8	V
Output Voltage	"H" Level	VOH	VIN=VIH	IOH=-100uA	3.3-5.0	3.1		V
					2.7-3.3	Vrom-0.2		
				IOH=-12mA	2.7	2.2		
				IOH=-18mA	3.0	2.4		
	"L" Level	VOL	VIN=VIL	IOL=30uA	2.7-5.0		0.2	
				IOL=12mA	2.7		0.4	
				IOL=18mA	3.0		0.4	

DC Characteristics(2.3V <= Vrom <= 2.7V) : Vrom is VDD pin voltage of ROM

Items		Symbol	Measurement Condition		Vrom(V)	Min.	Max.	Unit
Input Voltage	"H" Level	VIH			2.3-2.7	1.6	5.5	V
	"L" Level	VIL			2.3-2.7		0.8	V
Output Voltage	"H" Level	VOH	VIN=VIH	IOH=-100uA	2.3-2.7	Vrom-0.2		V
				IOH=-12mA	2.3	2.0		
				IOH=-18mA	2.3	1.8		
	"L" Level	VOL	VIN=VIL	IOL=40uA	2.3-2.7		0.2	
				IOL=12mA	2.3		0.4	
				IOL=18mA	2.3		0.6	

DC Characteristics(1.8V <= Vrom < 2.3V) : Vrom is VDD pin voltage of ROM

Items		Symbol	Measurement Condition		Vrom(V)	Min.	Max.	Unit
Input Voltage	"H" Level	VIH			1.8-2.3	1.6	5.5	V
	"L" Level	VIL			1.8-2.3		0.8	V
Output Voltage	"H" Level	VOH	VIN=VIH	IOH=-100uA	1.8-2.3	Vrom-0.2		V
				IOH=-6mA	1.8	1.4		
	"L" Level	VOL	VIN=VIL	IOL=60uA	1.8		0.2	
				IOL=6mA	1.8-2.3		0.3	

Remarks:

This specification is in the case that Extend-STD-16BIT-ROM Cable (CBL-STD-16-32) for RTE-100-TP is used alone or used with DIP40/42 Adapter.

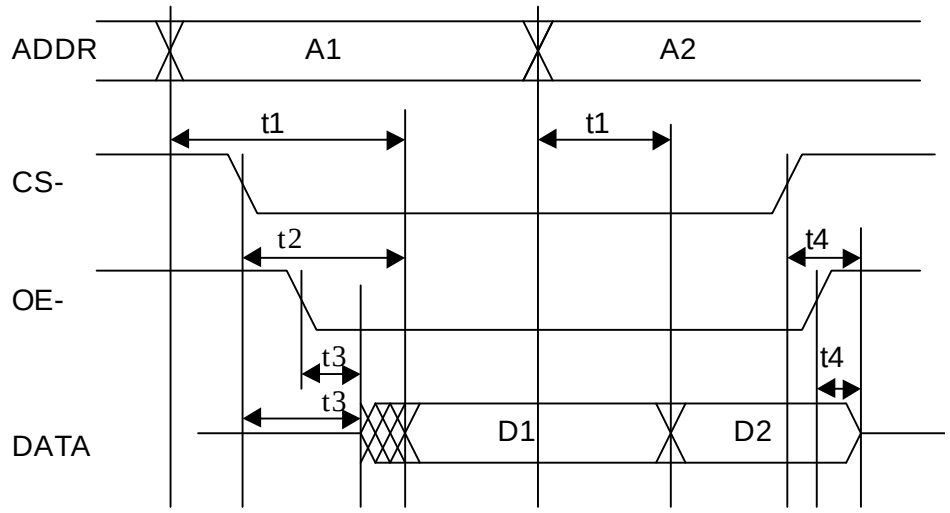
The characteristics that cable for RTE-100-TP (CBL-ROM32, CBL-ROM40, CBL-ROM42, CBL-STD16ROM) is used, is as follows.

The range of Vrom : 3.3 - 5.0V

VIL/VIH = TTL Level

VOH/VOL = 3.3V CMOS Level

ROM AC timing characteristics : READ cycle



Items	Symbols	Min.	Max.	Unit	Remarks
ADDR -> DATA	t1		35	nS	Access time from the address A0..A15
			40	nS	Access time from the address higher than or equal to A16
CS- -> DATA	t2		40	nS	Access time from the CS- active
CS-/OE- -> DATA	t3	8	24	nS	DATA output delay from CS- and OE- active
CS-/OE- -> DATA	t4		22	nS	DATA-Hiz delay from CS- or OE- inactive

Remarks:
This specification is in the case that Extend-STD-16BIT-ROM Cable (CBL-STD-16-32) for RTE-100-TP is used alone or used with DIP40/42 Adapter.
The characteristics that cable for RTE-100-TP (CBL-ROM32, CBL-ROM40, CBL-ROM42, CBL-STD16ROM) is used, is as follows.

Items	Symbols	Min.	Max.	Unit	Remarks
ADDR -> DATA	t1		50	nS	Access time from the address A0..A15
			50	nS	Access time from the address higher than or equal to A16
CS- -> DATA	t2		50	nS	Access time from the CS- active
CS-/OE- -> DATA	t3	10	40	nS	DATA output delay from CS- and OE- active
CS-/OE- -> DATA	t4		40	nS	DATA-Hiz delay from CS- or OE- inactive