KIT-NB85E-TP

User's Manual

RealTimeEvaluator

Software Version Up

* The latest RTE for Win32 (Rte4win32) can be down-loaded from following URL.

http://www.midas.co.jp/products/download/english/program/rte4win_32.htm

Notice

Trademarks

Revision History

Rev.0.8	Jul. 24, 1999	Preliminary 1st edition	
Rev.1.0	Sep. 24, 1999	Official 1st edition	The initial value of JTAG CLK changed to 12.5 MHz
Rev.2.0	Mar.4, 2000	2nd edition	Revised for supporting RTE-1000-TP
Rev.2.2	May.20, 2000	revised edition	Deleted 1 sentence in Precautions related to functions
Rev.2.3	Dec. 6,2000	revised	ENV commands are corrected.
Rev.2.4	May.20.2001	modified	download site

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1. OVERVIEW

KIT-NB85E-TP is the software to debug the system that has NEC RISC micro processor NB85E (ASIC-Core) by in-circuit emulation with RTE-100-TP or RTE-1000-TP.

This document describes how to use the KIT-NB85E-TP. Thus on using the product, please refer to the documents for RTE-100-TP or RTE-1000-TP also, that is main part of whole debugging system.

This product comes with the following components. First check that none of the components are missing.

- RTE for Win32 Setup Disk
- User's manual (This manual)
- License sheet

2. HARDWARE SPECIFICATIONS

Emulation

Target device				ASIC microcontroller using NB85E as core
RTE-TP				RTE-1000-TP
Emulation functions				
	Operating frequency			66 MHz (max.)
	Interface			JTAG/N-Wire
*4	JTAG clk			100 KHz - 25 MHz
Event function				
	Number of events			
		Setting of execution address		12
		Setting of data access		6
			Address specification	Maskable
			Data specification	Maskable
			Status specification	Maskable
			Number of sequential unit stages	4
Break functions				
	H/W break points			2
	S/W break points			100
	Breaks that can be set using events			Supported
	Step breaks			Supported
	Manual breaks			Supported
*4	Externall breaks			Supported
Trace functions				
	Trace data bus			4 bits
	Trace memory			4 bits x 128K words
	Trace delay			0 - 1FFFFh
*4	Trace clock			77 MHz (max.)
*4	Trace time tag			100 us - 30 h
	Trigger setting			Supported
		Trigger that can be set using an execution address		Supported
		Trigger setting by event		Supported
		Trigger setting by external input		Supported
	Start/stop by execution address			Supported
	Disassembled trace data display function			Provided
	Complete trace mode specification function			Provided (no real time)
ROM emulation functions				
*4	Memory capacity			8 M - 32 M-Byte
*4	Access time			40 ns (burst cycle:35sns)(*1)
*4	Operation voltage			1.8 - 5 V (*2)
*4	Electrical condition			LV-TTL (*3)
	Number of ROMs that can be emulated			
		DIP-32pin-ROM (8-bit ROM)		4 (max.)
		DIP-40/42pin-ROM (16-bit ROM)		2 (max.)
*4		Extend STD-16BIT-ROM connector		2 (max.)
	Types of ROMs that can be emulated			
		DIP-32-ROM probe (8bits-bus)		1M, 2M, 4M, 8M (27C010/020/040/080)
		DIP-40-ROM probe (16bits-bus)		1M, 2M, 4M (27C1024/2048/4096)
		DIP-42-ROM probe (16bits-bus)		8M, 16M (27C8000/16000)
*4		Extend STD-16BIT-ROM (16bits-bus)		1M, 2M, 4M, 8M, 16M, 16M, 32M, 64M, 128M, 256M
	Bus width specification (bits)			8/16/32
Pin mask functions				RESET, STOP, NMIx, VAREQ, WAIT-, INTxx

*1,2,3: These specifications are on the case using expansion 16bit standard ROM cable (CBL-STD16-32M) and DIP40/42 adapter.

*4: These specifications are on the case using RTE-1000-TP. For RTE-100-TP, please refer to the document of RTE-100-TP, as the specifications might differ from above.

3. RTE FOR WIN32

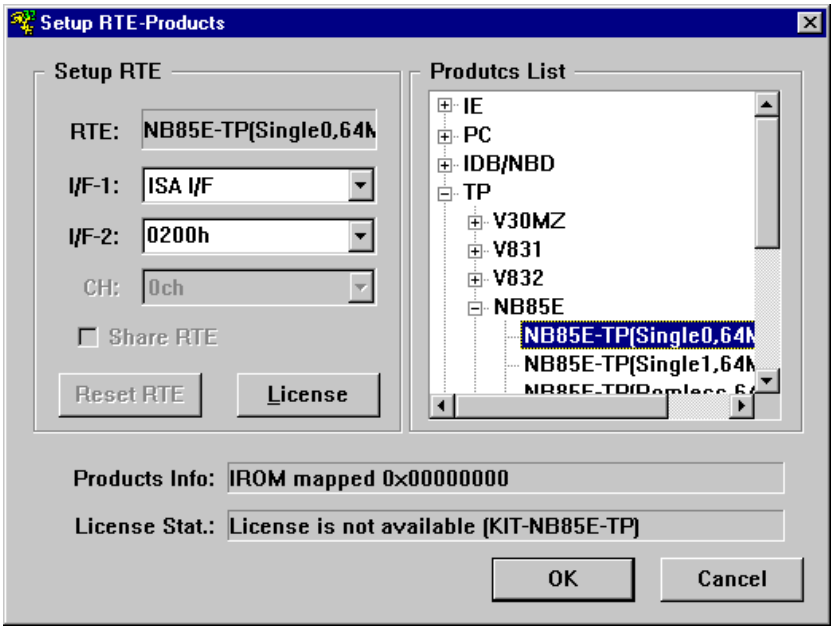
This chapter describes the setting of RTE for WIN32, with the focus on the aspects specific to KIT-NB85E-TP.

Invoking ChkRTE2.exe

After finishing to connect and apply the power supply for all equipments, invoke ChkRTE2.exe to setup the configuration of "RTEforWIN32".

Please setup the "RTEforWIN32" configuration at least one time for newly installed hardware.

<Setup RTE-Products>



<Selecting RTE>

From Product List, select the NB85E-TP(yyyy,xxxx) located beneath the TP tree. For yyyy, specify CPU operation mode, if and only if the evaluation system that has special RAM facilities for internal ROM emulation is used. Otherwise specify the item romless mode, regardlessly whether the CPU is implemented the mask ROM. The xxxx stands for CPU address mode.

<Selecting I/F-1, I/F-2>

Select and specify the host interface that suitable for your system from pull-down menu. (The display in example shows that RTE-PCAT is assigned to address 200h)

<License>

Click the button to setup license checking with the license setup sheet attached to the KIT package. For detail, please refer to the document of "RTE for WIN32".

<Function test>

If RTE-1000-TP is properly connected to the user system and capable of debugging, the following dialog box appears upon the normal completion of the function test. In this state, control from the debugger is possible.

If an error occurs during the test, the N-Wire cable is not properly connected. Check its connection.

Perform the ChkRTE2.exe function test after the RTE-100-TP or RTE-1000-TP has been connected to the user system and the power to all the devices has been turned on.

4. INITIALIZATION COMMANDS

Before debugging can be started, system initialization is required.

The following commands are available for system initialization, be sure to setup correctly before start to use the system.

To use Multi

Use following commands in Target window.

ENV command
* Setup port mask
* Specify JTAG clock
* Specify cache mode
* Specify CPU operation mode
* Others

ROM command
* Specify ROM emulation condition

NC/NCD command
* Specify data cache area for debugger software

NSPB/NSPBD command
* Specify forbid software break area

NROM/NROMD command
* Specify forced user area in rom emulation mapping area by ROM commad

To use PARTNER

Use following dialog.

Set CPU Environ dialog
* Setup port mask
* Specify JTAG clock
* Specify cache mode
* Specify CPU operation mode
* Others

Set Emulation ROM dialog
* Specify ROM emulation condition

NC/NCD command
* Specify data cache area for debugger software

NSPB/NSPBD command
* Specify forbid software break area

NROM/NROMD command
* Specify forced user area in rom emulation mapping area by ROM commad

Do not set cache operation mode to automatic (Auto), if the evaluation system with NB85E-TEG chip is not used. That might cause system malfunction for debugging capability.

5. INTERFACE SPECIFICATIONS

This chapter describes the specifications of the connectors used for control that are required for the user system.

Pin arrangement table

Pin number	Signal name	Input/output (user side)	Treatment (user side)
A1	CLKOUT	Output	22 - 33 Ω series resistor (recommended)
A2	TRCDATA0	Output	22 - 33 Ω series resistor (recommended)
A3	TRCDATA1	Output	22 - 33 Ω series resistor (recommended)
A4	TRCDATA2	Output	22 - 33 Ω series resistor (recommended)
A5	TRCDATA3	Output	22 - 33 Ω series resistor (recommended)
A6	TRCEND	Output	22 - 33 Ω series resistor (recommended)
A7	DDI	Input	10 kΩ pullup
A8	DCK	Input	10 kΩ pullup
A9	DMS	Input	10 kΩ pullup
A10	DDO	Output	22 - 33 Ω series resistor (recommended)
A11	DRST-	Input	10 kΩ pulldown
A12	DBINT	Output	10 kΩ pulldown
A13	NC.	------	Open

Pin number	Signal name	Input/output (user side)	Treatment (user side)
B1-B10	GND	------	Connection to the power GND
B11	NC.	------	Open
B12	NC.	------	Open
B13	+3.3V	------	Connection to the power

A12:DBINT : This capability is available only for RTE-1000-TP.
It detects the edge of signal that input to 1pin of EXT connector on main chassis of RTE-100-TP, then output break request to DBINT. The polarity of signal edge is configurable.

Connectors

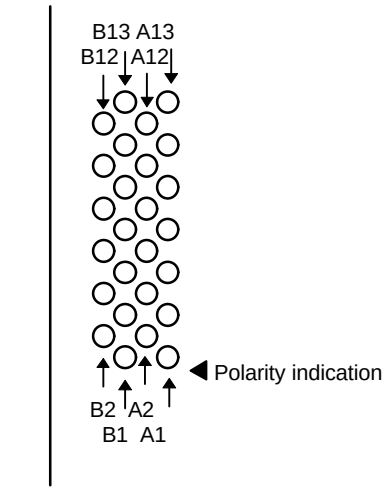
Manufacturer: KEL
Models: 8830E-026-170S (straight)
8830E-026-170L (right angle)
8831E-026-170L (right angle, fixing hardware attached)

Wiring on Target System

1.Keep the wire from the NB85E to the connector as short as possible.
>>100 mm or shorter is recommended.
2.Output signals from CPU are recommended to be connected to connectors, via high-speed CMOS buffers of which power supply is the same one with CPU I/O buffers.

Layout of the connectors on the board

The figure below shows the physical layout of the connectors on the board.



6. PRECAUTIONS

This chapter provides precautionary information on the use of KIT-NB85E-TP.

Precautions related to operation

1) Do not turn on the power to the user system while the power to KIT-NB85E-TP is off. Doing so can cause a malfunction.
2) KIT-NB85E-TP externally controls the debugging control circuit built into the NB85E. Consequently, KIT-NB85E-TP does not operate correctly unless the following conditions are satisfied:
   * KIT-NB85E-TP is properly connected to the user system using the N-Wire cable.
   * The power to the user system is on so that the NB85E can run correctly.

Precautions related to functions

1) The disassembly and display of real-time trace data is performed by reading the contents of memory at the point the trace display command is issued, according to the branching information received from the NB85E. Consequently, the disassembly and display of the program located in RAM of the user system is not correct if changes (including erroneous writing due to a CPU hang up) are made after program execution. Note that the following functional constraints must be observed.
2) If the trace information is limited by using the tron command, trace display may not be correctly performed. Therefore, specify all ON (start) or all OFF (stop) under normal conditions.
3) A breakpoint in the ROM space is invalid if the breakpoint is set to the second instruction of an instruction string that simultaneously execute two instructions.
4) For the CPU implemented on-chip cache, it is not possible to debug correctly during the cache is LOCK. If the cache is LOCK, the capabilities such as break, step execution or memory modification for corresponding memory region might malfunction.
5) For further information, be sure to refer to the Release Note of the KIT.