

KIT-V831/2-TP

User's Manual

RealTimeEvaluator

Software Version Up

* The latest RTE for Win32 (Rte4win32) can be down-loaded from following URL.

http://www.midas.co.jp/products/download/english/program/rte4win_32.htm

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Revision History

Rev.1.0	April 26,1997	1 st edition	
Rev.2.0	Mar.4,2000	2nd edition	Revised for supporting RTE-1000-TP
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1. OVERVIEW

KIT-V831/2-TP is the software to debug the system that has NEC RISC micro processor V831 and V832 by in-circuit emulation with RTE-100-TP or RTE-1000-TP.

This document describes how to use the KIT-V831/2-TP. Thus on using the product, please refer to the documents for RTE-100-TP or RTE-1000-TP also, that is main part of whole debugging system.

This product comes with the following components. First check that none of the components are missing.

- RTE for Win32 Setup Disk
- User's manual (This manual)
- License sheet

2. HARDWARE SPECIFICATIONS

Emulation

Target device		V831, V832
RTE-TP		RTE-1000-TP
Emulation functions		
	Operating frequency	V831:100MHz(max),V832:143MHz(max)
	Interface	JTAG/N-Wire
*4	JTAG clk	100 KHz - 25 MHz
Break functions		
	H/W break points	2
	S/W break points	100
	Breaks that can be set data access events	4
	Step breaks	Supported
	Manual breaks	Supported
Trace functions		
	Trace data bus	4 bits
	Trace memory	4 bits x 128K words
	Trace delay	0 - 1FFFFh
*4	Trace clock	77 MHz (max.)
*4	Trace time tag	100 us - 30 h
	Trigger setting	Supported
	Trigger that can be set using an execution address	1
*4	Trigger setting by data access events	2
	Trigger setting by external input	Supported
	Start by execution address	Supported
	Stop by execution address	Supported(V832 only)
	Disassembled trace data display function	Provided
	Data trace setting by data access events	2
	Complete trace mode specification function	Provided (no real time)
ROM emulation functions		
*4	Memory capacity	8 M - 32 M-Byte
*4	Access time	40 ns (burst cycle:35sns)(*1)
*4	Operation voltage	1.8 - 5 V (*2)
*4	Electrical condition	LV-TTL (*3)
	Number of ROMs that can be emulated	
	DIP-32pin-ROM (8-bit ROM)	4 (max.)
	DIP-40/42pin-ROM (16-bit ROM)	2 (max.)
*4	Extend STD-16BIT-ROM connector	2 (max.)
	Types of ROMs that can be emulated	
	DIP-32-ROM probe (8bits-bus)	1M, 2M, 4M, 8M (27C010/020/040/080)
	DIP-40-ROM probe (16bits-bus)	1M, 2M, 4M (27C1024/2048/4096)
	DIP-42-ROM probe (16bits-bus)	8M, 16M (27C8000/16000)
*4	Extend STD-16BIT-ROM (16bits-bus)	1M, 2M, 4M, 8M, 16M, 16M, 32M, 64M, 128M, 256M
	Bus width specification (bits)	8/16/32
Pin mask functions		INT00-03/10-13, NMI, RESET, HLDQR

*1,2,3: These specifications are on the case using expansion 16bit standard ROM cable (CBL-STD16-32M) and DIP40/42 adapter.

*4: These specifications are on the case using RTE-1000-TP. For RTE-100-TP, please refer to the document of RTE-100-TP, as the specifications might differ from above.

3. RTE FOR WIN32

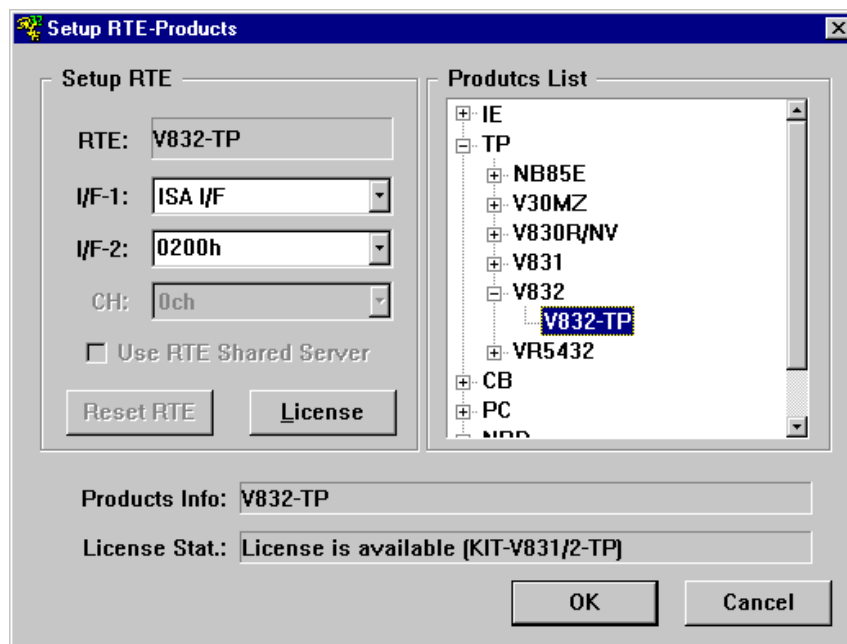
This chapter describes the setting of RTE for WIN32, with the focus on the aspects specific to KIT-V831/2-TP.

Invoking ChkRTE2.exe

After finishing to connect and apply the power supply for all equipments, invoke ChkRTE2.exe to setup the configuration of "RTEforWIN32".

Please setup the "RTEforWIN32" configuration at least one time for newly installed hardware.

<Setup RTE-Products>



<Selecting RTE>

From Product List, select the "V831-TP" or "V832-TP" located beneath the TP tree.

<Selecting I/F-1, I/F-2>

Select and specify the host interface that suitable for your system from pull-down menu. (The display in example shows that RTE-PCAT is assigned to address 200h)

<License>

Click the button to setup license checking with the license setup sheet attached to the KIT package. For detail, please refer to the document of "RTE for WIN32".

<Function test>

If RTE-1000-TP is properly connected to the user system and capable of debugging, the following dialog box appears upon the normal completion of the function test. In this state, control from the debugger is possible.



If an error occurs during the test, the N-Wire cable is not properly connected. Check its connection.



Perform the ChkRTE2.exe function test after the RTE-100-TP or RTE-1000-TP has been connected to the user system and the power to all the devices has been turned on.

4. INITIALIZATION COMMANDS

Before debugging can be started, system initialization is required.

The following commands are available for system initialization, be sure to setup correctly before start to use the system.

To use Multi

Use following commands in Target window.

ENV command

- * Setup port mask
- * Specify JTAG clock
- * Specify work area for accessing internal ram
- * Others

ROM command

- * Specify ROM emulation condition

NC/NCD command

- * Specify data cache area for debugger software

NSPB/NSPBD command

- * Specify forbid software break area

NROM/NROMD command

- * Specify forced user area in rom emulation mapping area by ROM command

To use PARTNER

Use following dialog.

Set CPU Environ dialog

- * Setup port mask
- * Specify JTAG clock
- * Specify work area for accessing internal ram
- * Others

Set Emulation ROM dialog

- * Specify ROM emulation condition

NC/NCD command

- * Specify data cache area for debugger software

NSPB/NSPBD command

- * Specify forbid software break area

NROM/NROMD command

- * Specify forced user area in rom emulation mapping area by ROM command

5. INTERFACE SPECIFICATIONS

This chapter describes the specifications of the connectors used for control that are required for the user system.

Pin arrangement table

Pin number	Signal name	Input/output (user side)	Treatment (user side)
A1	CLKOUT	Output	22 - 33 Ω series resistor (recommended)
A2	TRCDATA0	Output	22 - 33 Ω series resistor (recommended)
A3	TRCDATA1	Output	22 - 33 Ω series resistor (recommended)
A4	TRCDATA2	Output	22 - 33 Ω series resistor (recommended)
A5	TRCDATA3	Output	22 - 33 Ω series resistor (recommended)
A6	TRCEND	Output	22 - 33 Ω series resistor (recommended)
A7	DDI	Input	10 k Ω pullup
A8	DCK	Input	10 k Ω pullup
A9	DMS	Input	10 k Ω pullup
A10	DDO	Output	22 - 33 Ω series resistor (recommended)
A11	DRST-	Input	10 k Ω pulldown
A12	NC.	-----	Open
A13	NC.	-----	Open

Pin number	Signal name	Input/output (user side)	Treatment (user side)
B1-B10	GND	-----	Connection to the power GND
B11	NC.	-----	Open
B12	NC.	-----	Open
B13	+3.3V	-----	Connection to the power

Connectors

Manufacturer: KEL

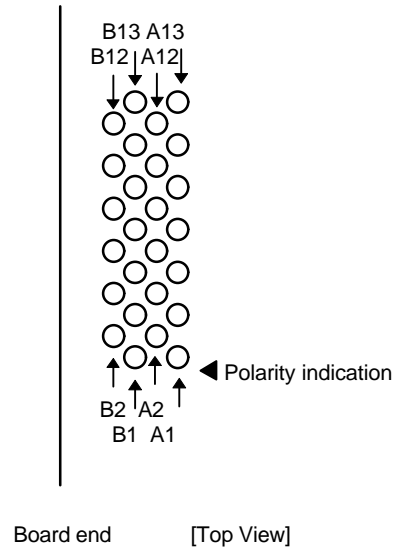
Models: 8830E-026-170S (straight)
8830E-026-170L (right angle)
8831E-026-170L (right angle, fixing hardware attached)

Wiring on Target System

1. Keep the wire from the NB85E to the connector as short as possible.
>>100 mm or shorter is recommended.
2. Output signals from CPU are recommended to be connected to connectors, via high-speed CMOS buffers of which power supply is the same one with CPU I/O buffers.

Layout of the connectors on the board

The figure below shows the physical layout of the connectors on the board.



6. PRECAUTIONS

This chapter provides precautionary information on the use of KIT-V831/2-TP.

Precautions related to operation

- 1) Do not turn on the power to the user system while the power to KIT-V831/2-TP is off. Doing so can cause a malfunction.
- 2) KIT-V831/2-TP externally controls the debugging control circuit built into the CPU. Consequently, KIT-V831/2-TP does not operate correctly unless the following conditions are satisfied:
 - * KIT-V831/2-TP is properly connected to the user system using the N-Wire cable.
 - * The power to the user system is on so that the CPU can run correctly.

Precautions related to functions

- 1) The disassembly and display of real-time trace data is performed by reading the contents of memory at the point the trace display command is issued, according to the branching information received from the CPU. Consequently, the disassembly and display of the program located in RAM of the user system is not correct if changes (including erroneous writing due to a CPU hang up) are made after program execution. Note that the following functional constraints must be observed.
 - a. Branch information may be overflowed when outputted from CPU.
When it changes into such a state, an analysis display cannot be carried out correctly.
 - b. When the output of a trace event is restricted, an analysis display cannot be carried out correctly.
- 2) It takes a break when a fatal exception occurs during user program execution.
After that, continuation is impossible.
- 3) Execution speed may become slow 10 or more times during trace in the full trace mode.
This is for a break to intervene frequently.
- 4) For further information, be sure to refer to the Release Note of the KIT.