<PRELIMINARY>

# KIT-VR4181A-TP

**User's Manual** 

RealTimeEvaluator

## Software Version Up

\* The latest RTE for Win32 (Rte4win32) can be down-loaded from following URL.

http://www.midas.co.jp/products/download/english/program/rte4win\_32.htm

#### Notice

\* The copyright associated with KIT-VR4181A-TP (including software and documentation) are proprietary to

Midas Lab. Co., Ltd.

\* This software and manual are protected under applicable copyright laws, and may not be copied, redistributed or modified in whole or in part, in any way without explicit prior written permission from Midas Lab. Co., Ltd.

\* The right of use granted for the customer means the right to use the software only on one system per one license. It is prohibited to use the one license of software on two or more systems at the same time.

\* While this product was manufactured with all possible care, Midas Lab. Co. Ltd. and its distributor assume

no responsibility whatsoever for any result of using the product.

\* The contents and specifications of this product and this document are subject to change without notice.

#### Trademarks

\* MS-Windows, Windows, MS and MS-DOS are the trademarks of Microsoft Corporation, U.S.A. The names of the programs, systems, CPUs, and other products that appear in this document are usually trademarks of the manufacturer of the corresponding product.

**Revision History** 

Rev.0.9 Dec. 24,2001

Preliminary 1st edition

# CONTENTS

	OVERVIEW4
2.	HARDWARE SPECIFICATIONS
	Emulation
3.	RTE FOR WIN32
	Invoking ChkRTE2.exe
4.	INITIALIZATION COMMANDS
	To use Multi
	To use PARTNER
5.	INTERFACE SPECIFICATIONS
	Pin arrangement table
	Connectors
	Wiring on Target System
	Layout of the connectors on the board10
6.	PRECAUTIONS11
	Precautions related to operation11
	Precautions related to functions11

# 1. OVERVIEW

**KIT-VR4181A-TP** is the software to debug the system that has NEC RISC micro processor VR4181A by in-circuit emulation with RTE-1000-TP.

This document describes how to use the KIT-VR4181A-TP. Thus on using the product, please refer to the documents RTE-1000-TP also, that is main part of whole debugging system.

This product comes with the following components. First check that none of the components are missing.

- RTE for Win32 Setup Disk
- User's manual (This manual)
- License sheet

# 2. HARDWARE SPECIFICATIONS

Emulation	

Target device			VR4181A	
RTE	TP		RTE-1000-TP	
Emulation functions				
	Оре	erating frequency	Unlimited	
	Inte	rface	JTAG/N-Wire	
	JTAG clk		100 KHz - 25 MHz	
Break functions		ctions		
	H/W	execution address break points	2	
	H/W	/ data access break points	2	
	S/W break points		100	
	Step breaks		Supported	
	Mar	ual breaks	Supported	
RON	ROM emulation functions			
	Memory capacity		8 M - 32 M-Byte	
	Access time		40 ns (burst cycle:35sns)(*1)	
	Operation voltage		1.8 - 5 V (*2)	
	Elec	trical condition	LV-TTL (*3)	
	Number of ROMs that can be emulated			
		DIP-32pin-ROM (8-bit ROM)	4 (max.)	
		DIP-40/42pin-ROM (16-bit ROM)	2 (max.)	
	Extend STD-16BIT-ROM connector Types of ROMs that can be emulated		2 (max.)	
		DIP-32-ROM probe (8bits-bus)	1M, 2M, 4M, 8M (27C010/020/040/080)	
		DIP-40-ROM probe (16bits-bus)	1M, 2M, 4M (27C1024/2048/4096)	
		DIP-42-ROM probe (16bits-bus)	8M, 16M (27C8000/16000)	
		Extend STD-16BIT-ROM (16bits-bus)	1M, 2M, 4M, 8M, 16M, 16M, 32M, 64M, 128M, 256M	
	Bus	width specification (bits)	8/16/32	
Pin ı	nask	functions	NMI, INTx, ColdResetB, ResetB	

\*1,2,3: These specifications are on the case using expansion 16bit standard ROM cable (CBL-STD16-32M) and DIP40/42 adapter.

### 3. RTE FOR WIN32

This chapter describes the setting of RTE for WIN32, with the focus on the aspects specific to KIT-VR4181A-TP.

#### Invoking ChkRTE2.exe

After finishing to connect and apply the power supply for all equipments, invoke ChkRTE2.exe to setup the configuration of "RTEforWIN32".

Please setup the "RTEforWIN32" configuration at least one time for newly installed hardware.

etup RTE	Produtcs List
RTE: VR4181A-TP(32Bit) I/F-1: ISA I/F I/F-2: 0200h CH: 0ch CH: 0ch CH: Ch: Shared Server Reset RTE License	<ul> <li>► V830R/NV</li> <li>► V831</li> <li>► V832</li> <li>► VR5432</li> <li>► VR4122</li> <li>■ NU85E</li> <li>■ VR5500</li> <li>■ VR4131</li> <li>■ VR4181A</li> <li>■ VR4181A</li> <li>■ VR4181A</li> <li>■ MIPS32_4Kc</li> <li>■ ADM/04550</li> </ul>

<Setup RTE-Products>

#### <Selecting RTE>

From Product List, select the "VR4181A-TP(32Bit)" located beneath the TP tree.

#### <Selecting I/F-1, I/F-2>

Select and specify the host interface that suitable for your system from pull-down menu. (The display in example shows that RTE-PCAT is assigned to address 200h)

#### <License>

Click the button to setup license checking with the license setup sheet attached to the KIT package. For detail, please refer to the document of "RTE for WIN32".

<Function test>

If RTE-1000-TP is properly connected to the user system and capable of debugging, the following dialog box appears upon the normal completion of the function test. In this state, control from the debugger is possible.

RTE for Windows	×
RTE function	al test
RTE functional test comp	leted successfully.
ОК	

If an error occurs during the test, the N-Wire cable is not properly connected. Check its connection.



Perform the ChkRTE2.exe function test after the RTE-1000-TP has been connected to the user system and the power to all the devices has been turned on.

# 4. INITIALIZATION COMMANDS

Before debugging can be started, system initialization is required.

The following commands are available for system initialization, be sure to setup correctly before start to use the system.

#### <u>To use Multi</u>

Use following commands in Target window.

ENV command

- \* Setup port mask
- \* Specify JTAG clock

\* Others

ROM command

\* Specify ROM emulation condition

NC/NCD command

\* Specify data cache area for debugger software

NSPB/NSPBD command

\* Specify forbid software break area

NROM/NROMD command

\* Specify forced user area in rom emulation mapping area by ROM command

#### To use PARTNER

Use following dialog.

Set CPU Environ dialog

- \* Setup port mask
- \* Specify JTAG clock
- \* Others

Set Emulation ROM dialog

\* Specify ROM emulation condition

NC/NCD command

\* Specify data cache area for debugger software

NSPB/NSPBD command

\* Specify forbid software break area

NROM/NROMD command

\* Specify forced user area in rom emulation mapping area by ROM command

# 5. INTERFACE SPECIFICATIONS

This chapter describes the specifications of the connectors used for control that are required for the user system.

#### Pin arrangement table

Pin number	Signal name	Input/output (user side)	Treatment (user side)
A1	NC.		Open or Connection to the GND
A2	NC.		Open or Connection to the GND
A3	NC.		Open or Connection to the GND
A4	NC.		Open or Connection to the GND
A5	NC.		Open or Connection to the GND
A6	NC.		Open or Connection to the GND
A7	RMODE/JTDI	Input	4.7k - 10 kΩ pullup
A8	JTCK	Input	4.7k - 10 kΩ pullup
A9	JTMS	Input	4.7k - 10 kΩ pullup
A10	JTDO	Output	22 - 33 $\Omega$ series resistor (recommended)
A11	JTRSTB	Input	4.7k - 10 kΩ pulldown
A12	BKTGIO_L	Input/Output	4.7k - 10 kΩ pullup
A13	NC.		Open

Pin number	Signal name	Input/output (user side)	Treatment (user side)
B1-B10	GND		Connection to the power GND
B11	NC.		Open
B12	NC.		Open
B13	+3.3V		Connection to the power

#### **Connectors**

Manufacturer: KEL Models: 8830E-026-170S (straight) 8830E-026-170L (right angle) 8831E-026-170L (right angle, fixing hardware attached)

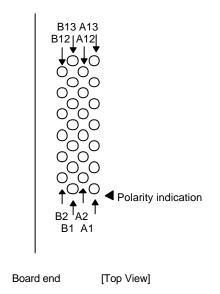
#### Wiring on Target System

- 1.Keep the wire from the CPU to the connector as short as possible. >>100 mm or shorter is recommended.
- 2.Output signals from CPU are recommended to be connected to connectors, via high-speed CMOS buffers of which power supply is the same one with CPU I/O buffers.

## KIT-VR4181A-TP

#### Layout of the connectors on the board

The figure below shows the physical layout of the connectors on the board.



# 6. PRECAUTIONS

This chapter provides precautionary information on the use of KIT-VR4181A-TP.

#### Precautions related to operation

- 1) Do not turn on the power to the user system while the power to RTE-1000-TP is off. Doing so can cause a malfunction.
- RTE-1000-TP externally controls the debugging control circuit built into the CPU Consequently, RTE-1000-TP does not operate correctly unless the following conditions are satisfied:
  - \* RTE-1000-TP is properly connected to the user system using the N-Wire cable.
  - \* The power to the user system is on so that the CPU can run correctly.
- 3) At the time of ICE use, in a target, when RTCRST# signal is a low, it is required for a NWIREEN pin to be "1."

#### Precautions related to functions

- 1) Don't LOCK cache. When it LOCKs, neither break in the area, nor step execution and rewriting of a memory can be performed normally.
- 2) Although RESET command and INIT command are commands which reset CPU, CPU internal device is not reset in the reset from commands.
- 3) For further information, be sure to refer to the Release Note of the KIT.