KIT-VR5500-TP

User's Manual

RealTimeEvaluator

Software Version Up

* The latest RTE for Win32 (Rte4win32) can be down-loaded from following URL.

http://www.midas.co.jp/products/download/english/program/rte4win_32.htm

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Revision History

Rev.1.00	May 5, 2001	Official 1st edition

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1. OVERVIEW

KIT-VR5500-TP is the software to debug the system that has NEC RISC micro processor VR5500 by in-circuit emulation with RTE-1000-TP.

This document describes how to use the KIT-VR5500-TP. Thus on using the product, please refer to the documents for RTE-1000-TP also, that is main part of whole debugging system.

This product comes with the following components. First check that none of the components are missing.

- RTE for Win32 Setup Disk
- User's manual (This manual)
- License sheet

2. HARDWARE SPECIFICATIONS

Emulation

Target device			VR5500
RTE-TP			RTE-1000-TP
Emulation functions			
	Operating frequency		---
	Interface		JTAG/N-Wire
	JTAG clk		100 KHz - 25 MHz
Break functions			
	H/W break points(*1)		1
	Breaks that can be set using access event(*2)		1
	S/W break points		100
	Step breaks		Supported
	Manual breaks		Supported
Trace functions(*3)			
	Trace data bus		4 bits
	Trace memory		4 bits x 128K words
	Trace delay		0 - 1FFFFh
	Trace clock		77 MHz (max.)
	Trace time tag		100 us - 30 h
	Trigger setting		Supported
		Trigger that can be set using an execution address(*1)	1
		Trigger setting by access event(*2)	1
		Trigger setting by external input	1
	Disassembled trace data display function		Provided
ROM emulation functions			
	Memory capacity		8 M - 32 M-Byte
	Access time		40 ns (burst cycle:35sns)(*4)
	Operation voltage		1.8 - 5 V (*5)
	Electrical condition		LV-TTL (*6)
	Number of ROMs that can be emulated		
		DIP-32pin-ROM (8-bit ROM)	4 (max.)
		DIP-40/42pin-ROM (16-bit ROM)	2 (max.)
		Extend STD-16BIT-ROM connector	2 (max.)
	Types of ROMs that can be emulated		
		DIP-32-ROM probe (8bits-bus)	1M, 2M, 4M, 8M (27C010/020/040/080)
		DIP-40-ROM probe (16bits-bus)	1M, 2M, 4M (27C1024/2048/4096)
		DIP-42-ROM probe (16bits-bus)	8M, 16M (27C8000/16000)
		Extend STD-16BIT-ROM (16bits-bus)	1M, 2M, 4M, 8M, 16M, 16M, 32M, 64M, 128M, 256M
	Bus width specification (bits)		8/16/32
Pin mask functions			NMI, INT

*1. The execution address event for a break and triggers is combination.
*2. The access event for a break and triggers is combination.
*3. Execution speed falls during trace.
*4,5,6: These specifications are on the case using expansion 16bit standard ROM cable (CBL-STD16-32M)
and DIP40/42 adapter.

3. RTE FOR WIN32

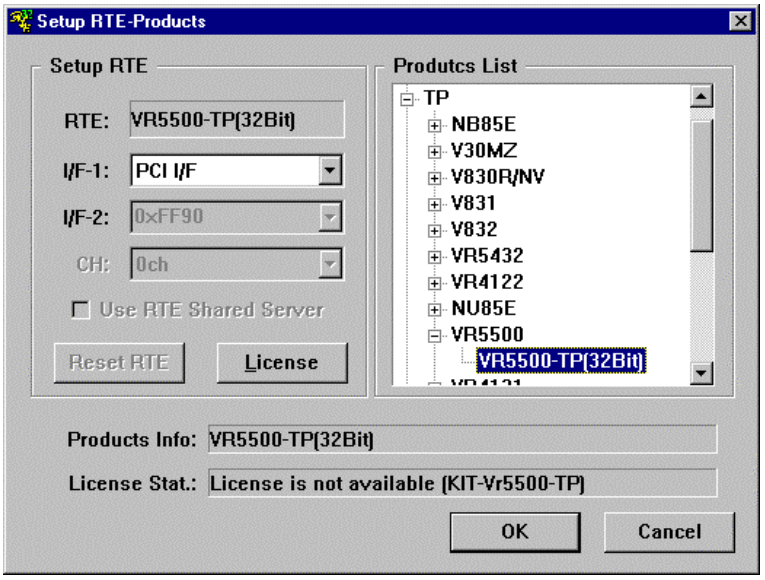
This chapter describes the setting of RTE for WIN32, with the focus on the aspects specific to KIT-VR5500-TP.

Invoking ChkRTE2.exe

After finishing to connect and apply the power supply for all equipments, invoke ChkRTE2.exe to setup the configuration of "RTEforWIN32".

Please setup the "RTEforWIN32" configuration at least one time for newly installed hardware.

<Setup RTE-Products>



<Selecting RTE>

From Product List, select the "VR5500-TP[xxxx]" located beneath the TP tree.

<Selecting I/F-1, I/F-2>

Select and specify the host interface that suitable for your system from pull-down menu. (The display in example shows that RTE-PCIIF is assigned)

<License>

Click the button to setup license checking with the license setup sheet attached to the KIT package. For detail, please refer to the document of "RTE for WIN32".

<Function test>

If RTE-1000-TP is properly connected to the user system and capable of debugging, the following dialog box appears upon the normal completion of the function test. In this state, control from the debugger is possible.

If an error occurs during the test, the N-Wire cable is not properly connected. Check its connection.

Perform the ChkRTE2.exe function test after the RTE-1000-TP has been connected to the user system and the power to all the devices has been turned on.

4. INITIALIZATION COMMANDS

Before debugging can be started, system initialization is required.
The following commands are available for system initialization, be sure to setup correctly before start to use the system.

To use Multi

Use following commands in Target window.

ENV command
* Setup port mask
* Specify JTAG clock
* Specify work area for cash processing
* Specify the high-speed download mode
* Others

ROM command
* Specify ROM emulation condition

NC/NCD command
* Specify data cache area for debugger software

NSPB/NSPBD command
* Specify forbid software break area

NROM/NROMD command
* Specify forced user area in rom emulation mapping area by ROM commad

To use PARTNER

Use following dialog.

Set CPU Environ dialog
* Setup port mask
* Specify JTAG clock
* Specify work area for cash processing
* Specify the high-speed download mode
* Others

Set Emulation ROM dialog
* Specify ROM emulation condition

NC/NCD command
* Specify data cache area for debugger software

NSPB/NSPBD command
* Specify forbid software break area

NROM/NROMD command
* Specify forced user area in rom emulation mapping area by ROM commad

5. INTERFACE SPECIFICATIONS

This chapter describes the specifications of the connectors used for control that are required for the user system.

Pin arrangement table

Pin number	Signal name	Input/output (user side)	Treatment (user side)
A1	CLKOUT	Output	22 - 33 Ω series resistor (recommended)
A2	TRCDATA0	Output	22 - 33 Ω series resistor (recommended)
A3	TRCDATA1	Output	22 - 33 Ω series resistor (recommended)
A4	TRCDATA2	Output	22 - 33 Ω series resistor (recommended)
A5	TRCDATA3	Output	22 - 33 Ω series resistor (recommended)
A6	TRCEND	Output	22 - 33 Ω series resistor (recommended)
A7	DDI	Input	4.7k - 10 kΩ pullup
A8	DCK	Input	4.7k - 10 kΩ pullup
A9	DMS	Input	4.7k - 10 kΩ pullup
A10	DDO	Output	22 - 33 Ω series resistor (recommended)
A11	DRST-	Input	4.7k - 50 kΩ pulldown
A12	Rmode*/ BkTGIO*	Input/Output	4.7k - 10 kΩ pullup
A13	NC.	------	Open

Pin number	Signal name	Input/output (user side)	Treatment (user side)
B1-B10	GND	------	Connection to the power GND
B11	NC.	------	Open
B12	NC.	------	Open
B13	+3.3V	------	Connection to the power

A11: Open or It connects ColdReset* via an external circuit with VR5500 ES1.1.
This signal is negative logic.

Connectors

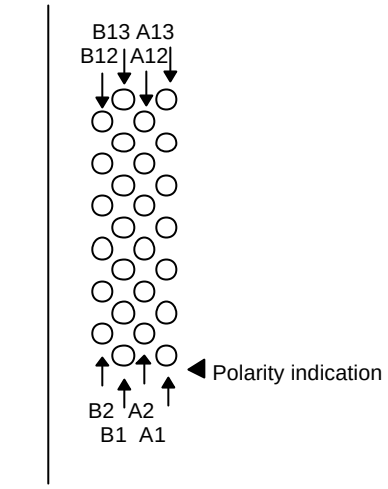
Manufacturer: KEL
Models: 8830E-026-170S (straight)
8830E-026-170L (right angle)
8831E-026-170L (right angle, fixing hardware attached)

Wiring on Target System

1.Keep the wire from the CPU to the connector as short as possible.
>>100 mm or shorter is recommended.
2.Output signals from CPU are recommended to be connected to connectors, via high-speed CMOS buffers of which power supply is the same one with CPU I/O buffers.

Layout of the connectors on the board

The figure below shows the physical layout of the connectors on the board.



6. PRECAUTIONS

This chapter provides precautionary information on the use of KIT-VR5500-TP.

Precautions related to operation

1) Do not turn on the power to the user system while the power to KIT-VR5500-TP is off. Doing so can cause a malfunction.
2) KIT-VR5500-TP externally controls the debugging control circuit built into the CPU Consequently, KIT-VR5500-TP does not operate correctly unless the following conditions are satisfied:
   * KIT-VR5500-TP is properly connected to the user system using the N-Wire cable.
   * The power to the user system is on so that the CPU can run correctly.

Precautions related to functions

1) It is related with real-time trace.
   * The disassemble display of real-time trace is performed by reading the contents of a memory on the basis of the branch information from CPU. Therefore, when the contents of a memory are changed after execution, the right execution history cannot be displayed. Moreover, when an error is in branch information, an analysis display cannot be done correctly.
   * When it runs from a break point one instruction of an execution start address does not write into trace.
   * Trace is automatically ended on condition that the following.
     - When the trigger point was passed and a break is taken.
     - When a break is taken in the state of the delay mode.
2) Don't LOCK cache. When it LOCKs, neither break in the area, nor step execution and rewriting of a memory can be performed normally.
3) For further information, be sure to refer to the Release Note of the KIT.
4) The following is the limitation in the case of doing ICE of VR5500 ES1.1.
   * The section about N-Wire in the limitation document of NEC Corp. issue corresponds to the limitation at the time of ICE use. Please use it after confirmation.
   * When trace is done from immediately after execution , a packet unnecessary one line is displayed just before execution. This should be disregarded. It is the line of the following (a).

Cycle	Sub	Address	Code	Instruction	EXT	Stat	
+000001	----	--------	--------	1 Count	1111	NSEQ	<< (a)
+000004	----	bfc00000	0bf00100	j bfc00400	1111	TPC	
+00000f	----	bfc00004	00000000	nop	1111	NSEQ	
+000012	----	bfc00400	40806800	mtc0 r0,$13	1111	NSEQ	