KIT-NB85E-TP

User's Manual (Rev.3.14)

RealTimeEvaluator

Software Version Up

* The latest RTE for Win32 (Rte4win32) can be down-loaded from following URL.
  http://www.midas.co.jp/products/download/english/program/rte4win_32.htm

Notice

Trademarks

REVISION HISTORY

Rev.0.80	Jul. 24, 1999	Preliminary 1st edition	
Rev.1.00	Sep. 24, 1999	Official 1st edition	The initial value of JTAG CLK changed to 12.5 MHz
Rev.2.00	Mar. 4, 2000	2nd edition	Revised for supporting RTE-1000-TP
Rev.2.20	May 20, 2000	Revised edition	Deleted 1 sentence in Precautions related to functions
Rev.2.30	Dec. 6, 2000	Revised	ENV commands are corrected.
Rev.2.40	May 20, 2001	Modified	download site
Rev.3.00	Nov. 22, 2001	3rd edition	Addition resulting from supporting RTE-2000-TP
Rev.3.01	Dec. 27, 2001	Revised	Addition of parameter wren to ROMx command
Rev.3.10	Apr. 27, 2002	Revised	Addition related to support of NU85E
Rev.3.12	Aug. 02, 2002	Revised	Clerical error correction * example of nrom/nromd commads * signals of Pin mask functions * nmi parameters of env command
Rev.3.13	Nov. 15, 2002	Revised	The following, * Chapter 2 Notes(*6) are added. * Chapter 3 Changed Screen of Chkrte2.exe * Chapter 5,6 the treatment of user side
Rev.3.14	May 12, 2003	Revised	The command added from Rte4win32 V5.10.xx is added. * Added command:eva/eve/evt/seq * added chapter 8 Clerical error correction * Correction of the number of events in Chapter 2.

CONTENTS

1. OVERVIEW

KIT-NB85E-TP is the software that performs in-circuit emulation for systems that have NEC RISC micro processor Nx85E (ASIC-Core) for debugging purposes. The hardware that can be used is RTE-100-TP, RTE-1000-TP, and RTE-2000-TP.

This manual describes how to use the KIT-NB85E-TP. Thus on using the product, please refer to the RTE-XXXX-TP Hardware User's Manual also, that is main part of whole debugging system.

This product comes with the following components. First check that none of the components are missing.

- RTE for Win32 (Rte4win32) Setup Disk
- User's manual (This manual)
- License sheet

2. HARDWARE SPECIFICATIONS

Emulation

Target device				ASIC microcontroller using Nx85E and DCU	
RTE-TP format to be used				RTE-1000-TP	RTE-2000-TP
JTAG-IF cable				Standard cable	RTE-NEC/MICTOR38
Emulation functions					
	CPU operating frequency			100KHz - (*6)	
	Interface			JTAG/N-Wire	
*4	Operation voltage			1.8 - 5 V (*2)	
*4	JTAG clk			100 kHz - 25 MHz	
Event function					
	Number of events				
		Setting of execution address		8	
		Setting of data access		4	
			Address specification	Maskable	
			Data specification	Maskable	
			Status specification	Maskable	
			Number of sequential unit stages	4	
Break functions					
	Hardware break points			2	
	Software break points			100	
	Breaks that can be set using events			Supported	
	Step breaks			Supported	
	Manual breaks			Supported	
*4	External breaks (High/Low edge)			Supported	
Trace functions					
	Trace data bus			4 bits	
	Trace memory			4 bits × 128k words	4 bits × 256k words
	Trigger setting			Supported	
		Trigger that can be set using an execution address		Supported	
		Trigger setting by data access		Supported	
		Trigger setting by event		Supported	
		Trigger setting by external input		Supported	
	Start/stop by execution address			Supported	
	Trace delay			0 - 1FFFFh	0 - 3FFFF
*4	Trace clock			77 MHz (max.)	133 MHz (max.)
*4	Time tag			100 ns - 30 h	
	Disassembled trace data display function			Provided	
	Complete trace mode specification function (no real time)			Provided	
ROM emulation functions (*5)					
*4	Map function in block (USER/EMEM)			None	64k words
*4	Used as RAM			Not supported	Supported
*4	Memory capacity			8M - 32M bytes	8M - 128M bytes
*4	Access time (():burst cycle)			40 ns (35 ns) (*1)	35 ns (30 ns) (*1)
*4	Operation voltage			1.8 - 5 V (*2)	
*4	Electrical condition			LV-TTL, 5-V tolerant (*3)	
	Number of ROMs that can be emulated				
		DIP-32pin-ROM (8-bit ROM)		4 (max.)	
		DIP-40/42pin-ROM (16-bit ROM)		2 (max.)	4 (max.)
*4		Extend STD-16BIT-ROM connector		2 (max.)	4 (max.)
	Sizes of ROMs that can be emulated (bits)				
		DIP-32-ROM (8-bit bus)		1M, 2M, 4M, 8M (27C010/020/040/080)	
		DIP-40-ROM (16-bit bus)		1M, 2M, 4M (27C1024/2048/4096)	
		DIP-42-ROM (16-bit bus)		8M, 16M (27C8000/16000)	
*4		Extend STD-16BIT-ROM (16-bit bus)		1M, 2M, 4M, 8M, 16M, 32M, 64M, 128M, 256M (32M bytes)	

	Bus width specification (bits)	8/16/32	8/16/32
Pin mask functions		RESET, STOP, NMIx, HLDRQ	

*1, 2, 3: Values when RTE-1000-TP + CBL-STD16-32M or RTE-2000-TP + CBL-STD16-2K is used.

*2: Note that the DC characteristics of each cable may not electrically match when the supply voltage is 2.3 V or less.

*4: For RTE-100-TP, please refer to the manual of RTE-100-TP, as the specifications might differ from above.

*5: Up to four E.MEM boards can be mounted to RTE-2000-TP, and the maximum capacity is 128M bytes. Two E.MEM boards are necessary for the 32-bit width, and four are necessary for the 64-bit width. One board is necessary per ROM with an 8-bit bus width.

*6. Please contact us, if you use it below 100kHz.

3. RTE for WIN32

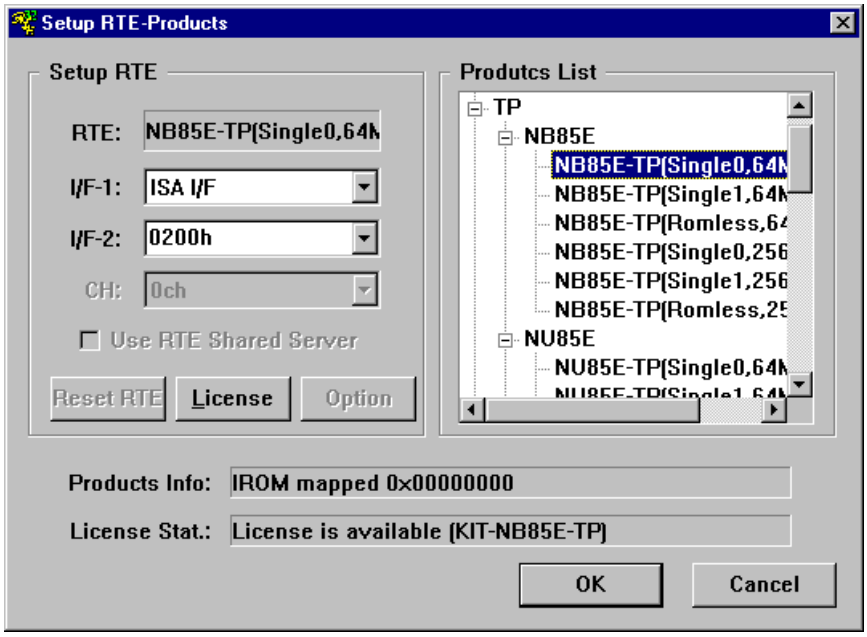
This chapter describes the setting of RTE for WIN32.

Invoking ChkRTE2.exe

After finishing to connect to the user system and apply the power supply for all equipments, invoke ChkRTE2.exe to set up the configuration of "RTE for WIN32".

Please set up the "RTE for WIN32" configuration at least one time for newly installed hardware.

<Setup RTE-Products>



<Selecting RTE>

From Product List, select the NB85E-TP(yyyy,xxxx) or NU85E-TP(yyyy.xxxx) located beneath the TP tree according with the CPU core type.

For yyyy, specify CPU operation mode, only if the evaluation system that has special RAM facilities for internal ROM emulation is used. Otherwise specify the item in romless mode, regardless of whether the CPU is implemented the mask ROM.

The xxxx stands for CPU address mode.

<Selecting I/F-1, I/F-2>

Select and specify the host interface that suitable for your system from pull-down menu. (The display in example shows that RTE-PCAT is assigned to address 200h.)

<License>

Click the button to set up license checking with the license setup sheet attached to the KIT package. For details, please refer to the manual of "RTE for WIN32".

NU85E-TP is supported by rte4win32 ver.5.06 or later.

<Function test>

If RTE for WIN32 is properly connected to the user system and capable of debugging, the following dialog box appears upon the normal completion of the function test. In this state, control from the debugger is possible.

If an error occurs during the test, the user system has a failure or the JTAG-IF cable is not properly connected. Check its connection.

Perform the ChkRTE2.exe function test after the RTE-xxxx-TP has been connected to the user system and the power to all the devices has been turned on.

4. INITIALIZATION COMMANDS

Before debugging can be started, system initialization is required, depending on hardware of the user system.

The following commands are available for system initialization. Be sure to set up correctly before start to use the system.

To use Multi

Use the following commands in Target window.

ENV command
* Specify pin mask.
* Specify JTAG clock.
* Specify cache mode.
* Specify CPU operation mode.
* Others

ROM command
* Specify ROM emulation condition.

NC/NCD command
* Specify data cache area for debugger.

NSPB/NSPBD command
* Specify forbid software break area.

NROM/NROMD command
* Specify forced user area.

To use PARTNER

Use the following dialog boxes.

CPU Environ dialog
* Specify pin mask.
* Specify JTAG clock.
* Specify cache mode.
* Specify CPU operation mode.
* Others

Emulation ROM dialog
* Specify ROM emulation condition.

NC/NCD command
* Specify data cache area for debugger.

NSPB/NSPBD command
* Specify forbid software break area.

NROM/NROMD command
* Specify forced user area.

Do not set cache operation mode to automatic (Auto), if the evaluation system with NB85E-TEG chip is not used. That might cause system malfunction for debugging capability.

5. INTERFACE SPECIFICATIONS: CONVENTIONAL TYPE (KEL)

The signal connections of the conventional type (KEL) JTAG/N-Wire interface are listed below.

Use of the high-speed interface explained in the next chapter is recommended for new designing.

Signal connection list

Pin number	Connected signal name	Input/output (user side)	Treatment (user side)
A1	TRCCLK	Output	22 - 33 Ω series resistor (recommended)
A2	TRCDATA0	Output	22 - 33 Ω series resistor (recommended)
A3	TRCDATA1	Output	22 - 33 Ω series resistor (recommended)
A4	TRCDATA2	Output	22 - 33 Ω series resistor (recommended)
A5	TRCDATA3	Output	22 - 33 Ω series resistor (recommended)
A6	TRCEND	Output	22 - 33 Ω series resistor (recommended)
A7	DDI	Input	4.7 k - 10 kΩ pullup
A8	DCK	Input	4.7 k - 10 kΩ pullup
A9	DMS	Input	4.7 k - 10 kΩ pullup
A10	DDO	Output	22 - 33 Ω series resistor (recommended)
A11	DRST-	Input	4.7 - 50 kΩ pulldown
A12	DBINT	Input	4.7 - 50 kΩ pulldown
A13	NC.	------	Open

Pin number	Connected signal name	Input/output (user side)	Treatment (user side)
B1-B10	GND	------	Connection to the GND
B11	NC.	------	Open
B12	NC.	------	Open
B13	VCCIO	------	Connection to the I/O power supply (+3.3 V normally)

I/O (user side): Input/output direction at the user board side

A12-DBINT: The edge of the signal input to RTE-XXXX-TP main enclosure pin 1 of EXT connector: RSV-INO is detected and a break request is output to DBINT. The direction of the edge can be specified. (RTE-100-TP is not supported.)

B13-VCCIO: Directly connect a power supply for I/O of the device that is to interface with the corresponding signal.

For details of the connectors and wiring, refer to the manual of RTE-XXXX-TP.

6. INTERFACE SPECIFICATIONS: HIGH-SPEED TYPE (MICTOR)

The signal connections of the high-speed (MICTOR) JTAG/N-Wire interface are listed below.

This interface is supported by RTE-2000-TP only.

Signal connection list

Pin number	Connected signal name	Input/output (user side)	Treatment (user side)
1	GND		Connection to the GND
3(A8)	DCK	Input	4.7 k - 10 kΩ pullup or pulldown
5(A9)	DMS	Input	4.7 k - 10 kΩ pullup or pulldown
7(A7)	DDI	Input	4.7 k - 10 kΩ pullup or pulldown
9(A10)	DDO	Output	22 - 33 Ω series resistor (recommended)
11	---	---	Open
13	---	---	Open
15	---	---	Open
17(A1)	TRCCLK	Output	22 - 33 Ω series resistor (recommended)
19(A6)	TRCEND	Output	22 - 33 Ω series resistor (recommended)
21(A2)	TRCDATA0	Output	22 - 33 Ω series resistor (recommended)
23(A3)	TRCDATA1	Output	22 - 33 Ω series resistor (recommended)
25(A4)	TRCDATA2	Output	22 - 33 Ω series resistor (recommended)
27(A5)	TRCDATA3	Output	22 - 33 Ω series resistor (recommended)
29	---	---	Open or GND
31	---	---	Open or GND
33	---	---	Open or GND
35	---	---	Open or GND
37	GND		Connection to the GND

Pin number	Connected signal name	Input/output (user side)	Treatment (user side)
2	GND		Connection to the GND
4(B13)	VCCIO	---	Connection to the I/O power supply of CPU (for power monitoring)
6(A11)	DRST-	Input	4.7 k - 50 kΩ pulldown
8(A12)	DBINT	Input	4.7 k - 50 kΩ pulldown
10(A13)	---	---	Open
12	---	---	Open
14(B11)	(EVTTRG)	Output	22 - 33 Ω series resistor (recommended)
16(B12)	---	---	Open
18	---	---	Open
20	---	---	Open
22	---	---	Open or GND
24	---	---	Open or GND
26	---	---	Open or GND
28	---	---	Open or GND
30	---	---	Open or GND
32	---	---	Open or GND
34	---	---	Open or GND
36	---	---	Open or GND
38	GND	---	Connection to the GND

Remark: ( ) indicates an equivalent pin of the KEL type connector.

I/O (user side) indicates the input/output direction at the user board side.

Pin 14 (EVTTRG) is unused.

7. PRECAUTIONS

This chapter provides precautionary information on the use of KIT-NB85E-TP.

Precautions related to operation

1) Do not turn on the power to the user system while the power to KIT-NB85E-TP is off. Doing so can cause a malfunction.
2) KIT-NB85E-TP externally controls the debugging control circuit (DCU) built into the CPU. Consequently, KIT-NB85E-TP does not operate correctly unless the following conditions are satisfied:
   * KIT-NB85E-TP is properly connected to the user system using the JTAG-IF cable.
   * The power to the user system is on so that the CPU can run correctly.

Precautions related to functions

1) The disassembly display of real-time trace data is performed by reading the contents of memory at the point the trace display command is issued, according to the branching information received from the CPU. Consequently, the disassembly display of the program located in RAM of the user system is not correct if changes (including erroneous writing due to a CPU hang up) are made after program execution.
2) If the trace information is limited, trace display may not be correctly performed. Therefore, usually use the initial values (all traces are output).
3) A breakpoint in the ROM space is invalid if the breakpoint is set to the second instruction of an instruction string that simultaneously execute two instructions.
4) For the CPU implemented on-chip cache, it is not possible to debug correctly during the cache is locked. If the cache is locked, the capabilities such as break, step execution, or memory modification for corresponding memory region might malfunction.
5) For further information, be sure to refer to the Release Note of the KIT.

8. DETAILS OF TRACE FUNCTIONS

This appendix describes the real-time trace function.

Overview of the trace function

The real-time trace function writes the details of the execution (trace data) output from the CPU in the trace buffer in the ICE for each execution. You can check the data using the trace command.

You can set the trace mode, trace start condition, trigger condition, section condition, qualify condition, and other conditions to specify the loading of trace data.

For the flow of loading trace data, see Figures 1 and 2.

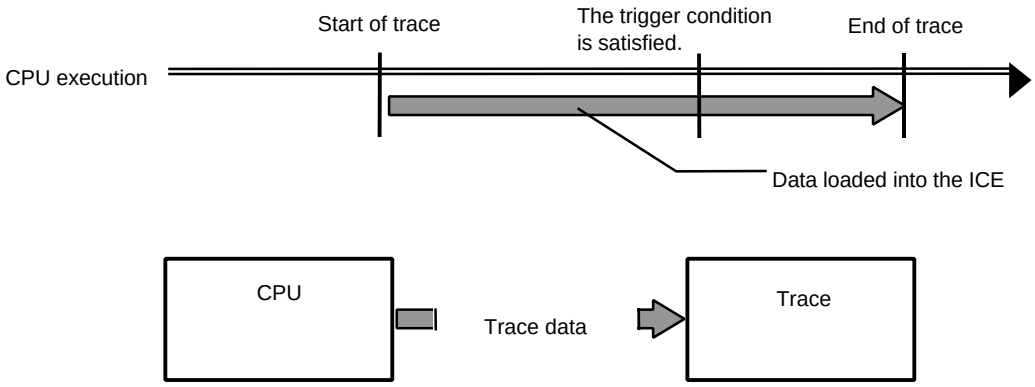


Figure 1 Flow of loading trace data

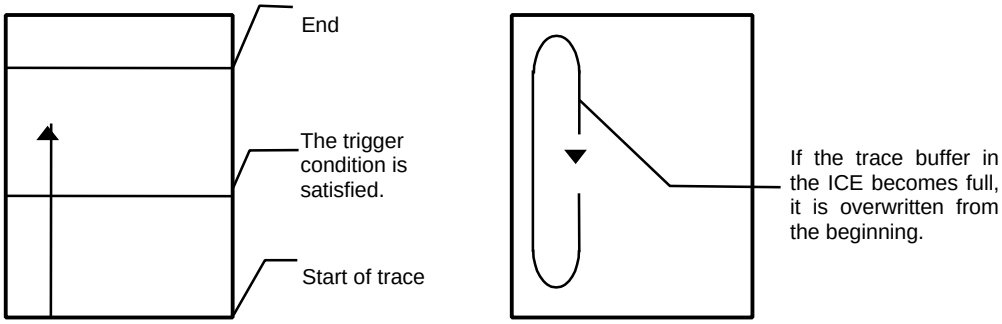


Figure 2 Trace data in the ICE

Delay count

The delay count means the number of cycles in which trace data is to be loaded after the trigger condition is satisfied (Figure 3). The number of cycles differs depending on the type of CPU execution. One cycle is not one execution unit.

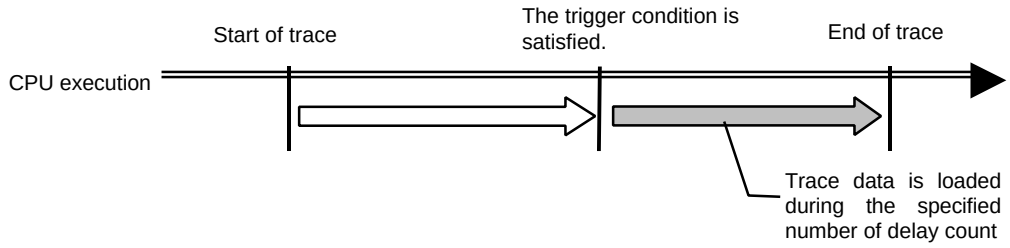


Figure 3 Flow of delay count

Trace execution mode

In **the real-time mode**, trace data is loaded with priority given to the CPU execution. If the trace buffer (FIFO) in the CPU becomes full, part of trace data may not be loaded (Figure 4).

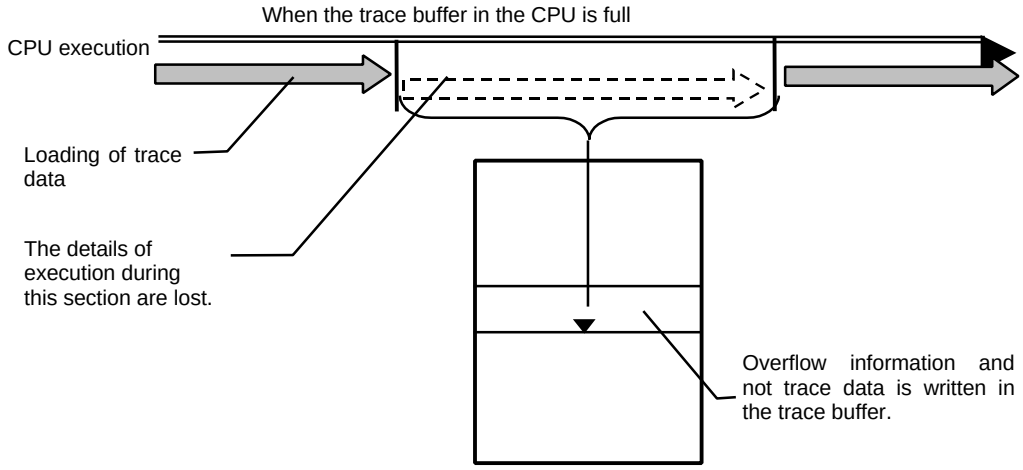


Figure 4 Real-time mode

In **the non-real-time mode**, all trace data can be loaded. If the trace buffer (FIFO) in the CPU becomes full in this mode, the CPU execution is temporarily stopped and is automatically restarted (Figure 5).

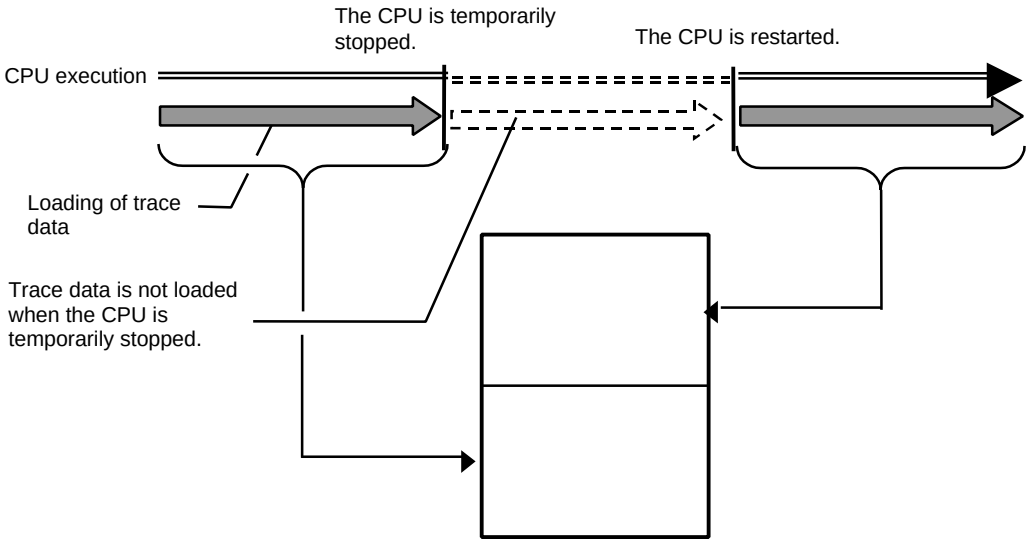


Figure 5 Non-real-time mode

Starting trace

To start loading trace data, the following methods are available (Figure 6)

In order to use trace switch point 1 for a start condition, "tr1_all" needs to be set up of the tron command.

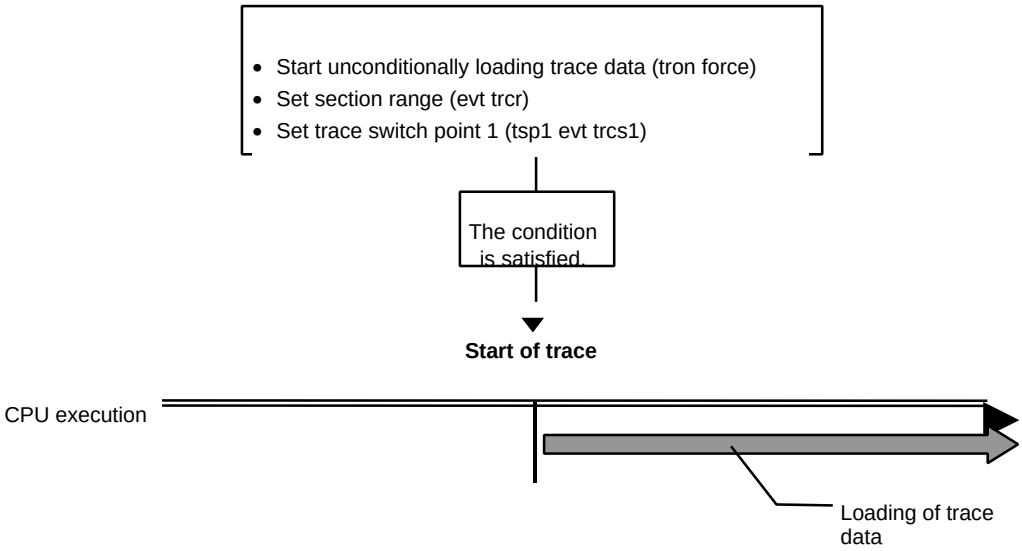


Figure 6 Starting trace

Trigger condition

A trigger condition is used as the start point of delay count (Figure 7). You can set a trigger condition to check the details of the execution before and after the trigger.

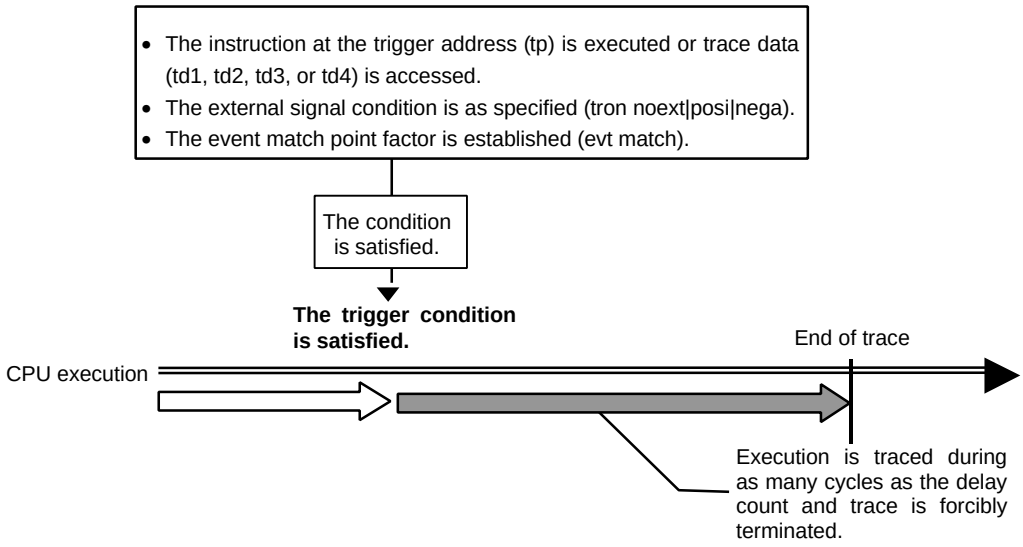


Figure 7 Trigger condition

Stopping trace

To stop loading trace data, the following methods are available.(Figure 8)

In order to use trace switch point 2 for a stop condition, "tr2_" needs to be set up of the tron command.

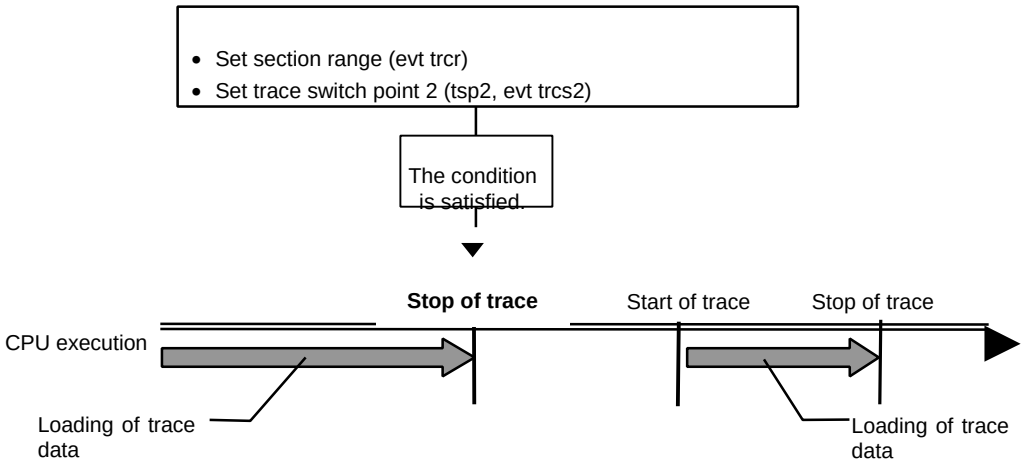


Figure 8 Stopping trace

Terminating trace

After trace is terminated, no more trace data is loaded.(Figure 9).

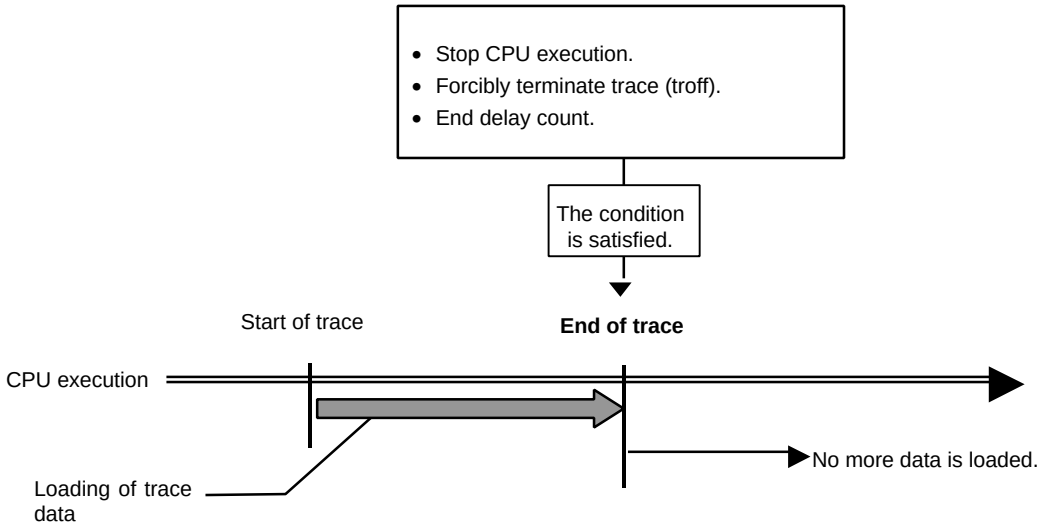


Figure 9 Terminating trace

Forced delay mode

In the forced delay mode, trace is forcibly terminated when trace data is loaded during the specified delay count (number of cycles) after the start of trace. In this mode, the trigger condition is ignored (Figure 10). When CPU execution starts, trace is started in this mode.

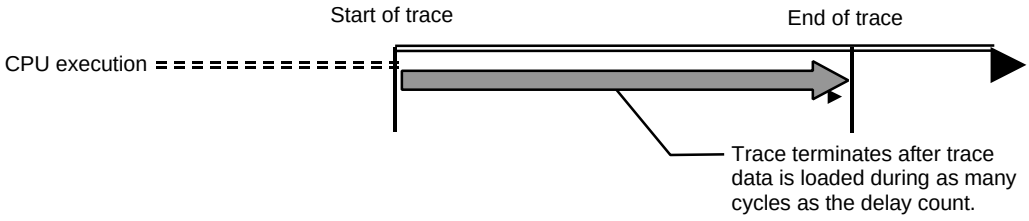


Figure 10 Forced delay mode