KIT-V850E/MA3-TP

User's Manual (Rev.1.02)

RealTimeEvaluator

Software Version Up

* The latest RTE for Win32 (Rte4win32) can be down-loaded from following URL.

    http://www.midas.co.jp/products/download/english/program/rte4win_32.htm

Notice

Trademarks

REVISION HISTORY

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Rev.1.00	Nov. 13, 2002	Official 1st edition
Rev.1.01	Feb. 8, 2003	The following additions are made:
		* MODE1 connection is added to "Interface Specifications".
		* "Others" is added to "Precautions".
Rev1.02	Apr. 25, 2003	The description about the function of the following added and changed by Rte4win32 V5.10.xx is added.
		* The number of the break points which can be used in the Internal ROM space is extended to 6 from 2.
		* Description of the added IFROMxxx command is added to Appendix .A.

CONTENTS

1. OVERVIEW

KIT-V850E/MA3-TP is the software that performs in-circuit emulation for systems that have NEC RISC micro processor V850E/MA3 for debugging purposes. The hardware that can be used is RTE-1000-TP and RTE-2000-TP.

This manual describes how to use the KIT-V850E/MA3-TP. Thus on using the product, please refer to the RTE-XXXX-TP Hardware User's Manual also, that is main part of whole debugging system.

This product comes with the following components. First check that none of the components are missing.

- RTE for Win32 (Rte4win32) Setup CD-ROM
- User's manual (This manual)
- License sheet

2. HARDWARE SPECIFICATIONS

<u>**Emulation**</u>

Target device		V850E/MA3	
RTE-TP format to be used		RTE-1000-TP	RTE-2000-TP
JTAG-IF cable		Standard cable	RTE-NEC/MICTOR38
Emulation functions			
*6	CPU operating frequency	At least 100 kHz	
	Interface	JTAG/N-Wire	
	Operation voltage	1.8 - 5 V (*2)	
	JTAG CLK	100 kHz - 25 MHz	
Break functions			
	Hardware breakpoints	2	
*5	Software breakpoints	100(Internal ROM area is limited to 4 points)	
	Step breaks	Supported	
	Manual breaks	Supported	
ROM emulation functions (*4)			
	Map function in block (USER/EMEM)	None	64k words
	Used as RAM	Not supported	Supported
	Memory capacity	8M - 32M bytes	8M - 128M bytes
	Access time ((): burst cycle)	40 ns (35 ns) (*1)	35 ns (30 ns) (*1)
	Operation voltage	1.8 - 5 V (*2)	
	Electrical condition	LV-TTL, 5-V tolerant (*3)	
	Number of ROMs that can be emulated		
	DIP-32pin-ROM (8-bit ROM)	4 (max.)	
	DIP-40/42pin-ROM (16-bit ROM)	2 (max.)	4 (max.)
	Extend STD-16BIT-ROM connector	2 (max.)	4 (max.)
	Sizes of ROMs that can be emulated (bits)		
	DIP-32-ROM (8-bit bus)	1M, 2M, 4M, 8M (27C010/020/040/080)	
	DIP-40-ROM (16-bit bus)	1M, 2M, 4M (27C1024/2048/4096)	
	DIP-42-ROM (16-bit bus)	8M, 16M (27C8000/16000)	
	Extend STD-16BIT-ROM (16-bit bus)	1M, 2M, 4M, 8M, 16M, 32M, 64M, 128M, 256M (32M bytes)	
	Bus width specification (bits)	8/16/32	8/16/32
Pin mask functions		NMI, INTWDG, WAIT-, HLDRQ, RESET-	

Execution time measurement function (the value when the JTAGCLK frequency is 25 MHz is shown in parentheses.)
  Resolution (ns)
  Maximum measurement time (ns)
		t = doubled JTAGCLK frequency (80 ns)
		$t*2^{32}$ (about 171 s)	

*1, 2, 3: Values when RTE-1000-TP + CBL-STD16-32M or RTE-2000-TP + CBL-STD16-2K is used.

*2: Note that the DC characteristics of each cable may not electrically match when the supply voltage is 2.3 V or less.

*4: Up to four E.MEM boards can be mounted to RTE-2000-TP, and the maximum capacity is 128M bytes. Two E.MEM boards are necessary for the 32-bit width, and four are necessary for the 64-bit width. One board is necessary per ROM with an 8-bit bus width.

*5: The number of software breakpoints that can be set depends on the debugger.

*6. Please contact us, if you use it below 100 kHz.

3. RTE for WIN32

This chapter describes the setting of RTE for WIN32.

<u>**Invoking ChkRTE2.exe**</u>

After finishing to connect to the user system and apply the power supply for all equipments, invoke ChkRTE2.exe to set up the configuration of "RTE for WIN32".

Please set up the "RTE for WIN32" configuration at least one time for newly installed hardware.

<Setup RTE-products>

<Selecting RTE>
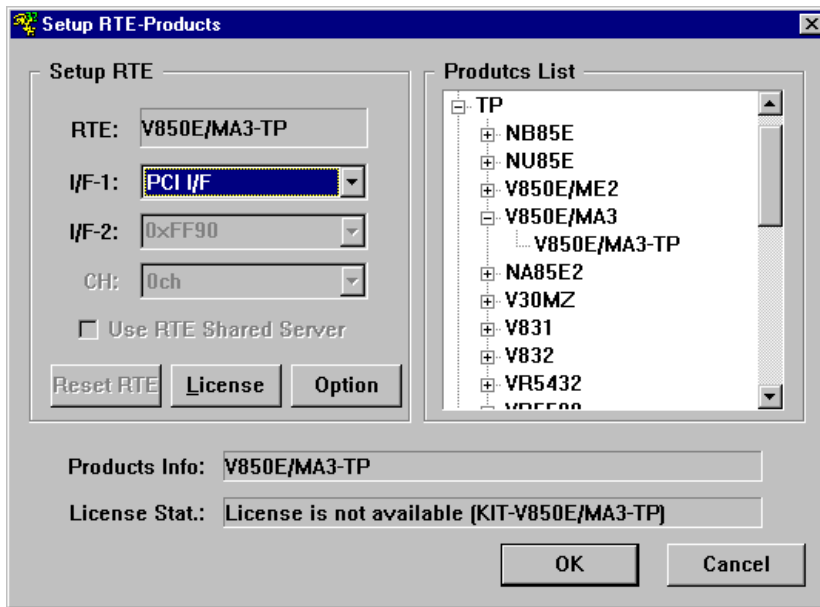
From Product List, select the V850E/MA3-TP located beneath the TP tree.

<Selecting I/F-1, I/F-2>

Select and specify the host interface that suitable for your system from pull-down menu. (The display in example shows that PCI-Card is assigned)

<License>

Click the button to set up license checking with the license setup sheet attached to the KIT package. For details, please refer to the manual of "RTE for WIN32".

<Option>

Click the button to enter the security ID code.

<Initial status>

The following shows each address of the ID code in the ROM and its corresponding field and an example of input. In this example, items 0x11, 0x22, 0x33, and so on are input in the corresp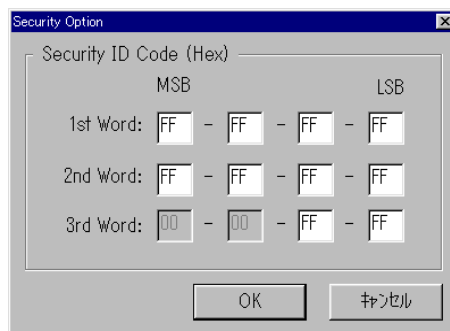onding fields, starting with the field corresponding to address 0x70. After changing the ID code, be sure to change the values on this Option screen to the same values.

0x73 0x77   0x70 0x74 0x78

<Input example>
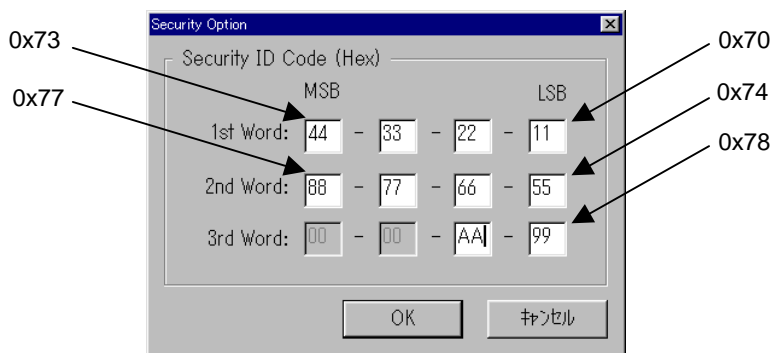
Security function for the internal ROM/flash memory
To start the debugger, the 10-byte ID code must be authenticated. An overview of the ID code is given below. For the details, refer to the manual of the CPU.

- **The ID code is indicated by the 10-byte data at addresses 0x70 to 0x79.**
- **Bit 7 at address 0x79 is the ICE connection enable flag. To connect an ICE, this bit must be set to 1.**
- **If the ID code input on this Option screen does not match the ID code in the internal ROM/flash memory, the debugger is not started.**
- **When the flash memory is erased, the ID code is 0xFFFFFFFFFFFFFFFFFFFF.**

V850E/MA3-TP is supported by rte4win32 ver.5.07 or later.
The version to recommend is 5.10.xx.

<Function test>

For the function test RTE for WIN32 must properly be connected to the user system and identified by the ID code. If you set up RTE and then perform a function test according to the screen instructions, the following dialog box appears upon the normal completion of the function test. In this state, control from the debugger is possible.

```
┌─────────────────────────────────────────────────────────┐
│ RTE for Windows                                      [X] │
├─────────────────────────────────────────────────────────┤
│                                                           │
│                   RTE functional test                    │
│                                                           │
│          RTE functional test completed successfully.     │
│                                                           │
│                      ┌──────────┐                         │
│                      │    OK    │                         │
│                      └──────────┘                         │
└─────────────────────────────────────────────────────────┘
```

If an error occurs during the test, the user system has a failure or the JTAG-IF cable is not properly connected. Check its connection.

> ⚠ **Perform the ChkRTE2.exe function test after the RTE-xxxx-TP has been connected to the user system and the power to all the devices has been turned on.**

4. INITIALIZATION COMMANDS

Before debugging can be started, system initialization is required, depending on hardware of the user system.

The following commands are available for system initialization. Be sure to set up correctly before start to use the system.

<u>**To use Multi**</u>

Use the following commands in the target window.

ENV command
   * Specify pin mask.
   * Specify JTAG clock.
   * Others
ROM command
   * Specify ROM emulation condition.
NC/NCD command
   * Specify data cache area for debugger.
NSPB/NSPBD command
   * Specify forbid software break area.
NROM/NROMD command
   * Specify forced user area.

<u>**To use PARTNER**</u>

Use the following dialog boxes.

CPU Environ dialog
   * Specify pin mask.
   * Specify JTAG clock.
   * Others
Emulation ROM dialog
   * Specify ROM emulation condition.
NC/NCD command
   * Specify data cache area for debugger.
NSPB/NSPBD command
   * Specify forbid software break area.
NROM/NROMD command
   * Specify forced user area.

5. INTERFACE SPECIFICATIONS: CONVENTIONAL TYPE (KEL)

The signal connections of the conventional type (KEL) JTAG/N-Wire interface are listed below.

> ⚠️ **Use of the high-speed interface explained in the next chapter is recommended for new designing.**

Signal connection list

Pin number	Connected signal name	Input/output (user side)	Treatment (user side)
A1	(TRCCLK)	Output	Open or GND
A2	(TRCDATA0)	Output	Open or GND
A3	(TRCDATA1)	Output	Open or GND
A4	(TRCDATA2)	Output	Open or GND
A5	(TRCDATA3)	Output	Open or GND
A6	(TRCEND)	Output	Open or GND
A7	DDI	Input	4.7 k - 10 kΩ pullup
A8	DCK	Input	4.7 k - 10 kΩ pullup
A9	DMS	Input	4.7 k - 10 kΩ pullup
A10	DDO	Output	22 - 33 Ω series resistor (recommended)
A11	DRST-	Input	4.7 k - 50 kΩ pulldown
A12	(DBINT)	Input	Open
A13	MODE1	Input	4.7 k - 50 kΩ pulldown

Pin number	Connected signal name	Input/output (user side)	Treatment (user side)
B1-B10	GND	------	Connection to the GND
B11	NC.	------	Open
B12	NC.	------	Open
B13	VCCIO	------	Connection to the I/O power supply (+3.3 V normally)

I/O (user side):   Input/output direction at the user board side

B13-VCCIO: Directly connect a power supply for I/O of the device that is to interface with the corresponding signal.

Pins whose connected signal names are enclosed in parentheses: Not used for the V850E/MA3.

> ⚠️ **For details of the connectors and wiring, refer to the manual of RTE-XXXX-TP.**

6. INTERFACE SPECIFICATIONS: HIGH-SPEED TYPE (MICTOR)

The signal connections of the high-speed (MICTOR) JTAG/N-Wire interface are listed below.

> ⚠️ **This interface is supported by RTE-2000-TP only.**

Signal connection list

Pin number	Connected signal name	Input/output (user side)	Treatment (user side)
1	GND		Connection to the GND
3(A8)	DCK	Input	4.7 k - 10 kΩ pullup
5(A9)	DMS	Input	4.7 k - 10 kΩ pullup
7(A7)	DDI	Input	4.7 k - 10 kΩ pullup
9(A10)	DDO	Output	22 - 33 Ω series resistor (recommended)
11	---	---	Open
13	---	---	Open
15	---	---	Open
17(A1)	(TRCCLK)	Output	Open or GND
19(A6)	(TRCEND)	Output	Open or GND
21(A2)	(TRCDATA0)	Output	Open or GND
23(A3)	(TRCDATA1)	Output	Open or GND
25(A4)	(TRCDATA2)	Output	Open or GND
27(A5)	(TRCDATA3)	Output	Open or GND
29	---	---	Open or GND
31	---	---	Open or GND
33	---	---	Open or GND
35	---	---	Open or GND
37	GND		Connection to the GND

Pin number	Connected signal name	Input/output (user side)	Treatment (user side)
2	GND		Connection to the GND
4(B13)	VCCIO	---	Connection to the I/O power supply of CPU (for power monitoring)
6(A11)	DRST-	Input	4.7 k - 50 kΩ pulldown
8(A12)	(DBINT)	Input	Open
10(A13)	MODE1	Input	4.7 k - 50 kΩ pulldown
12	---	---	Open
14(B11)	(EVTTRG)	Output	Open or GND
16(B12)	---	---	Open
18	---	---	Open
20	---	---	Open
22	---	---	Open or GND
24	---	---	Open or GND
26	---	---	Open or GND
28	---	---	Open or GND
30	---	---	Open or GND
32	---	---	Open or GND
34	---	---	Open or GND
36	---	---	Open or GND
38	GND	---	Connection to the GND

Remark: ( ) in the "Pin number" column indicates an equivalent pin of the KEL type connector.

I/O (user side) indicates the input/output direction at the user board side.

Pins whose connected signal names are enclosed in parentheses: Not used for the V850E/MA3.

7. PRECAUTIONS

This chapter provides precautionary information on the use of KIT-V850E/MA3-TP.

Precautions related to operation

1) Do not turn on the power to the user system while the power to KIT-V850E/MA3-TP is off. Doing so can cause a malfunction.

2) KIT-V850E/MA3-TP externally controls the debugging control circuit (DCU) built into the CPU. Consequently, KIT-V850E/MA3-TP does not operate correctly unless the following conditions are satisfied:
   * KIT-V850E/MA3-TP is properly connected to the user system using the JTAG-IF cable.
   * The power to the user system is on so that the CPU can run correctly.
   * The correct ID code is set. (see Chapter 3, "RTE for WIN32".)

Precautions related to functions

1) 2 points of hardware breakpoints are automatically used as breakpoints to internal ROM space. The break point to a total of six can be set to Intenal ROM space.

> **Precautions for using Multi**
> **Multi implicitly uses breakpoints in the following cases:**
> 1. **When Step, Next, Return, Come, and others are executed at the source level: Two points**
> 2. **When the execution is started immediately after downloading at the source level: One point**
> 3. **When the syscall function is used: One point (always)**
> **To debug a program stored in the internal ROM, take some measures so that the maximum number of set breakpoints is not also exceeded when the above points are included. If the maximum number is exceeded, the following error message appears:**
> **(0x87) Exhaust the number of settings**

> **Precautions for using PARTNER**
> **PARTNER implicitly uses breakpoints in the following cases:**
> 1. **When Step, Trace, Return, Come, and others are executed at the source level: Two points (max.)**
> 2. **When the syscall function is used: One point (always)**
> **To debug a program stored in the ROM, take some measures so that the maximum number of set breakpoints (2) is not also exceeded when the above points are included. If the maximum number is exceeded, an error message appears.**

2) A hardware breakpoint is invalid if the breakpoint is set to the second instruction of an instruction string that simultaneously execute two instructions.

3) Be sure to refer to the Release Note and other manuals if provided.

Limitations

There are the following limitations on the use of rte4win32 Ver 5.09.xx or older:

1) No data can be written (or downloaded) into the internal ROM.

2) The numbers of break points which can be set to Intetnal ROM space are only two hardware break points.

Others

1) Initializing the ASID register
   Before using the emulator, set the value of the ASID register to 0x00 for future compatibility. If the emulator is used with the ASID register set to other than 0x00, a break function may be disabled.

2) About a ROM collection function
   A ROM collection function cannot be used at the time of ICE connection.
   A ROM collection function is used by the ICE side for the software break function to a Internal ROM space. Since it is cleared by the reset to CPU, the break point using a ROM collection function becomes invalid after it, when reset is put into a user system during execution. It becomes again effective by rerunning after a break.

3) Do not use the self-programming function when an ICE is connected.