KIT-VR4120-TP

User's Manual (Rev.1.01)

RealTimeEvaluator

Software Version Up

* The latest RTE for Win32 (Rte4win32) can be down-loaded from following URL.
  http://www.midas.co.jp/products/download/english/program/rte4win_32.htm

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REVISION HISTORY

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1. OVERVIEW

KIT-VR4120-TP is the software that performs in-circuit emulation for systems that have NEC RISC micro processor VR4122 for debugging purposes. The hardware that can be used is RTE-1000-TP and RTE-2000-TP.

This manual describes how to use the KIT-VR4120-TP. Thus on using the product, please refer to the **RTE-XXXX-TP Hardware User's Manual** also, that is main part of whole debugging system.

This product comes with the following components. First check that none of the components are missing.

- RTE for Win32 (Rte4win32) Setup Disk
- User's manual (This manual)
- License sheet

2. HARDWARE SPECIFICATIONS

Emulation

Target device		VR4122(ES3.0 -) (*5)	
RTE-TP format to be used		RTE-1000-TP	RTE-2000-TP
JTAG-IF cable		Standard cable	RTE-NEC/MICTOR38
Emulation functions			
	Operating frequency	Unlimited	
	Interface	JTAG/N-Wire	
	Operation voltage	1.8 - 5 V (*2)	
	JTAG clk	100 kHz - 25 MHz	
Break functions			
	Break by execution address event	2	
	Break setting by access event	2	
	Software break points	100	
	Step breaks	Supported	
	Manual breaks	Supported	
Trace function		None	
ROM emulation functions			
	Map function in block (USER/EMEM)	None	In 64k-word units
	Used as RAM	Not supported	Supported
	Memory capacity	8M - 32M bytes	8M - 128M bytes (*4)
	Access time	40 ns (35 ns) (*1)	35 ns (30 ns) (*1)
	Operation voltage	1.8 - 5 V (*2)	
	Electrical condition	LV-TTL, 5-V tolerant (*3)	
	Number of ROMs that can be emulated		
	DIP-32pin-ROM (8-bit ROM)	4 (max.)	
	DIP-40/42pin-ROM (16-bit ROM)	2 (max.)	4 (max.)
	Extend STD-16BIT-ROM connector	2 (max.)	4 (max.)
	Sizes of ROMs that can be emulated (bits)		
	DIP-32-ROM (8-bit bus)	1M, 2M, 4M, 8M (27C010/020/040/080)	
	DIP-40-ROM (16-bit bus)	1M, 2M, 4M (27C1024/2048/4096)	
	DIP-42-ROM (16-bit bus)	8M, 16M (27C8000/16000)	
	Extend STD-16BIT-ROM (16-bit bus)	1M, 2M, 4M, 8M, 16M, 32M, 64M, 128M, 256M	
	Bus width specification (bits)	8/16/32	8/16/32/64
Pin mask functions		NMI, INT	

*1, 2, 3: Values when RTE-1000-TP + CBL-STD16-32M or RTE-2000-TP + CBL-STD16-2K is used.

*2: Note that the DC characteristics of each cable may not electrically match when the supply voltage is 2.3 V or less.

*4: Up to four E.MEM boards can be mounted to RTE-2000-TP, and the maximum capacity is 128M bytes. Two E.MEM boards are necessary for the 32-bit width, and four are necessary for the 64-bit width. One board is necessary per ROM with an 8-bit bus width.

*5. RTE-2000-TP does not support the VR4122 ES3.0.

3. RTE for WIN32

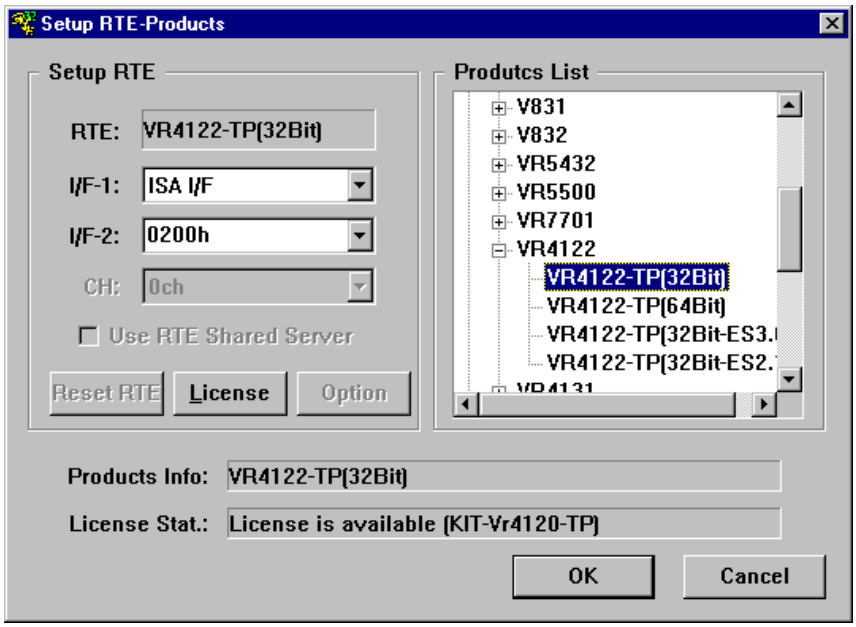
This chapter describes the setting of RTE for WIN32.

Invoking ChkRTE2.exe

After finishing to connect to the user system and apply the power supply for all equipments, invoke ChkRTE2.exe to set up the configuration of "RTE for WIN32".

Please set up the "RTE for WIN32" configuration at least one time for newly installed hardware.

<Setup RTE-Products>



<Selecting RTE>

From Product List, select the VR4122-TP(xxx) located beneath the TP tree.

VR4122-TP(32Bit) : Usually, please specify this.

VR4122-TP(64Bit) : Please specify to do a register display by 64-Bit width by MULTI.

VR4122-TP(32Bit-ES3.0) : Please specify, if you do ICE of ES3.0 of VR4122.

VR4122-TP(32Bit-ES2.1) : Please do not specify.

The targeted CPU is ES3.1 or later of the VR4122. To use ES3.0, see "Precautions related to the version of CPU (VR4122)" in Chapter 6. The CPU earlier than ES3.0 should not be used.

<Selecting I/F-1, I/F-2>

Select and specify the host interface that suitable for your system from pull-down menu. (The display in example shows that RET-PCAT is assigned to address 200h.)

<License>

Click the button to set up license checking with the license setup sheet attached to the KIT package. For details, please refer to the manual of "RTE for WIN32".

<Function test>

If RTE for WIN is properly connected to the user system and capable of debugging, the following dialog box appears upon the normal completion of the function test. In this state, control from the debugger is possible.

If an error occurs during the test, the user system has a failure or the JTAG/N-Wire cable is not properly connected. Check its connection.

Perform the ChkRTE2.exe function test after the RTE-xxxx-TP has been connected to the user system and the power to all the devices has been turned on.

4. INITIALIZATION COMMANDS

Before debugging can be started, system initialization is required, depending on hardware of the user system.

The following commands are available for system initialization. Be sure to set up correctly before start to use the system.

To use Multi

Use the following commands in Target window.

ENV command
* Specify pin mask.
* Specify JTAG clock.
* Others

ROM command
* Specify ROM emulation condition.

NC/NCD command
* Specify data cache area for debugger.

NSPB/NSPBD command
* Specify forbid software break area.

NROM/NROMD command
* Specify forced user area.

To use PARTNER

Use the following dialog boxes.

CPU Environ dialog
* Specify pin mask.
* Specify JTAG clock.
* Others

Emulation ROM dialog
* Specify ROM emulation condition.

NC/NCD command
* Specify data cache area for debugger.

NSPB/NSPBD command
* Specify forbid software break area.

NROM/NROMD command
* Specify forced user area.

5. INTERFACE SPECIFICATIONS

This chapter describes the specifications of the connectors used for the JTAG/N-Wire interface.

Pin arrangement table

Pin number	Signal name	Input/output (user side)	Treatment (user side)
A1	TRCCLK (*1)	Output	22 - 33 Ω series resistor (recommended)*1
A2	NC.	------	Open or GND
A3	NC.	------	Open or GND
A4	NC.	------	Open or GND
A5	NC.	------	Open or GND
A6	NC.	------	Open or GND
A7	RMODE/JTDI	Input	4.7 k - 10 kΩ pullup
A8	JTCK	Input	4.7 k - 10 kΩ pullup
A9	JTMS	Input	4.7 k - 10 kΩ pullup
A10	JTDO	Output	22 - 33 Ω series resistor (recommended)
A11	JTRSTB	Input	4.7 k - 10 kΩ pulldown
A12	BKTGIO_L	Input/Output	4.7 k - 10 kΩ pullup
A13	NC.	------	Open

Pin number	Signal name	Input/output (user side)	Treatment (user side)
B1-B10	GND	------	Connection to the GND
B11	NC.	------	Open
B12	NC.	------	Open
B13	+3.3V	------	Connection to the +3.3-V power

*1: It is required when CPU (VR4122) is ES3.0

Connectors

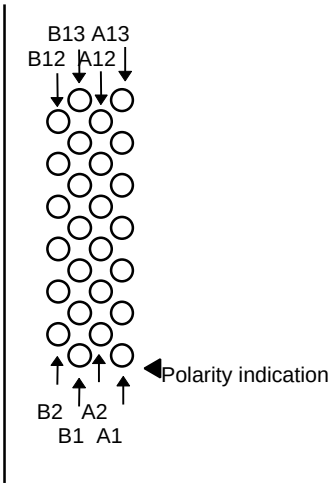
Manufacturer: KEL
Models: 8830E-026-170S (straight)
8830E-026-170L (right angle)
8831E-026-170L (right angle, fixing hardware attached)

Wiring on target system

1. Keep the wire from the CPU to the connector as short as possible.
   (100 mm or shorter is recommended.)
2. Output signals from CPU are recommended to be connected to connectors, via high-speed CMOS buffers of which power supply is the same one with CPU I/O buffers.

Layout of the connectors on the board

The figure below shows the physical layout of the connectors on the board.



Board end [Top View]

For details of the connectors and wiring, refer to the manual of RTE-XXXX-TP.

6. PRECAUTIONS

This chapter provides precautionary information on the use of KIT-VR4120-TP.

Precautions related to operation

1) Do not turn on the power to the user system while the power to KIT-VR4120-TP is off. Doing so can cause a malfunction.
2) KIT-VR4120-TP externally controls the debugging control circuit built into the CPU. Consequently, KIT-VR4120-TP does not operate correctly unless the following conditions are satisfied:
   * KIT-VR4120-TP is properly connected to the user system using the N-Wire cable.
   * The power to the user system is on so that the CPU can run correctly.
3) At the time of ICE use, in a target, when RTCRST# signal changes from a low level to a high level, it is required for a TRCEND/NWIREEN/HLDAK# pin to be "1."
   When it is impossible, please start ICE, before HALTIMER shutdown of CPU occurs (within four seconds after applying the power).

Precautions related to functions

1) This KIT corresponds to a 32-bit address space. It does not correspond to the address mode of 64-Bit.
2) A virtual address corresponds, only when TLB is in the state of always hitting statically.
3) A locked cache cannot be debugged. When the cache is locked, break in the area, step execution, or rewriting of a memory may not be performed normally.
4) The RESET command and INIT command from ICE do not reset the peripheral devices in the CPU.
5) For further information, be sure to refer to the Release Note of the KIT and the restrictions imposed by NEC.

Precautions related to the version of CPU (VR4122)

The CPU (VR4122) ES3 and earlier cannot be emulated.
To emulate VR4122 ES3 with an in-circuit emulator, use RTE-1000-TP, keeping the following points in mind.

1) Please choose VR4122-TP(32BIT-ES3) in the product set up by ChkRTE2.exe.
2) TRCCLK needs to be connected with A1 pin of a JTAG/N-Wire connector. This CPU pin cannot be used for any other purposes.
3) If an error occurs during connection test of ChkRTE2.exe, and an unstable operation such as a hang-up during debugging occurs, set switch No. 4 at the front end of RTE-1000-TP to ON if it is OFF, or to OFF if it is ON, whichever the operation may be stabilized.
4) The frequency of JTAG clock is 1/8 fixation of CPU operation clock of the VR4122.
   >> Even if the parameter of jtagxx is input in the ENV command, it is invalid.

RTE-2000-TP does not support versions of VR4122 earlier than ES3.1.