KIT-VR5500-TP

User's Manual(Rev.2.02)

RealTimeEvaluator

Software Version Up

* The latest RTE for Win32 (Rte4win32) can be down-loaded from following URL.

  http://www.midas.co.jp/products/download/english/program/rte4win_32.htm

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Revision History   2

Rev.1.00	May 5, 2001	Official 1st edition
Rev.2.00	Nov.15, 2002	2nd edition
		• Addition resulting from support of RTE-2000-TP, etc.
Rev.2.01	Apr. 25, 2003	VR5500A adds to an target device.
		• Chapter 2
Rev.2.02	Mar. 03, 2004	The following is added.
		• 7, 8th section of Chapter 7
		• The tclkdiv parameter of the env command

CONTENTS

1. OVERVIEW   4

    KIT-VR5500-TP is the software that performs in-circuit emulation for systems that have NEC RISC micro processor VR5500 for debugging purposes.   The hardware that can be used is RTE-1000-TP and RTE-2000-TP.

    This manual describes how to use the KIT-VR5500-TP.   Thus on using the product, please refer to the **RTE-XXXX-TP Hardware User's Manual** also, that is main part of whole debugging system.

    This product comes with the following components.   First check that none of the components are missing.

- RTE for Win32 (Rte4win32) Setup Disk
- User's manual (This manual)
- License sheet

2. HARDWARE SPECIFICATIONS

Emulation

Target device(*8)		VR5500, VR5500A	
RTE-TP format to be used		RTE-1000-TP	RTE-2000-TP
JTAG-IF cable		Standard cable	RTE-NEC/MICTOR38
Emulation functions			
	CPU operating frequency	Unlimited	
	Interface	JTAG/N-Wire	
	Operation voltage	1.8 - 5 V (*2)	
	JTAG clk	100 kHz - 25 MHz	
Break functions			
	H/W break points(*5)	1	
	Breaks that can be set using access event(*6)	1	
	S/W break points	100	
	Step breaks	Supported	
	Manual breaks	Supported	
Trace functions(*7)			
	Trace data bus	4 bits	
	Trace memory	4 bits × 128k words	4 bits × 256k words
	Trigger setting	Supported	
	Trigger that can be set using an execution address(*5)	1	
	Trigger setting by access event(*6)	1	
	Trigger setting by external input	1	
	Trace delay	0 - 1FFFFh	0 - 3FFFF
	Trace clock	77 MHz (max.)	133 MHz (max.)
	Time tag	100 ns - 30 h	
	Disassembled trace data display function	Provided	
ROM emulation functions (*4)			
	Map function in block (USER/EMEM)	None	64k words
	Used as RAM	Not supported	Supported
	Memory capacity	8M - 32M bytes	8M - 128M bytes
	Access time (( ): burst cycle)	40 ns (35 ns) (*1)	35 ns (30 ns) (*1)
	Operation voltage	1.8 - 5 V (*2)	
	Electrical condition	LV-TTL, 5-V tolerant (*3)	
	Number of ROMs that can be emulated		
	DIP-32pin-ROM (8-bit ROM)	4 (max.)	
	DIP-40/42pin-ROM (16-bit ROM)	2 (max.)	4 (max.)
	Extend STD-16BIT-ROM connector	2 (max.)	4 (max.)
	Sizes of ROMs that can be emulated (bits)		
	DIP-32-ROM (8-bit bus)	1M, 2M, 4M, 8M (27C010/020/040/080)	
	DIP-40-ROM (16-bit bus)	1M, 2M, 4M (27C1024/2048/4096)	
	DIP-42-ROM (16-bit bus)	8M, 16M (27C8000/16000)	
	Extend STD-16BIT-ROM (16-bit bus)	1M, 2M, 4M, 8M, 16M, 32M, 64M, 128M, 256M (32M bytes)	
	Bus width specification (bits)	8/16/32	8/16/32/64
Pin mask functions		NMI, INT	

*1, 2, 3: Values when RTE-1000-TP + CBL-STD16-32M or RTE-2000-TP + CBL-STD16-2K is used.

*2: Note that the DC characteristics of each cable may not electrically match when the supply voltage is 2.3 V or less.

*4: Up to four E.MEM boards can be mounted to RTE-2000-TP, and the maximum capacity is 128M bytes. Two E.MEM boards are necessary for the 32-bit width, and four are necessary for the 64-bit width. One board is necessary per ROM with an 8-bit bus width.

*5. The execution address event for a break and triggers is combination.

*6. The access event for a break and triggers is combination.

*7. Execution speed falls during trace.

*8. Rte4win32 V5.10.xx , or newer is required for VR5500A.

3. RTE FOR WIN32

This chapter describes the setting of RTE for WIN32, with the focus on the aspects specific to KIT-VR5500-TP.

Invoking ChkRTE2.exe

After finishing to connect and apply the power supply for all equipments, invoke ChkRTE2.exe to setup the configuration of "RTEforWIN32".

Please setup the "RTEforWIN32" configuration at least one time for newly installed hardware.

<Setup RTE-Products>

<Selecting RTE>
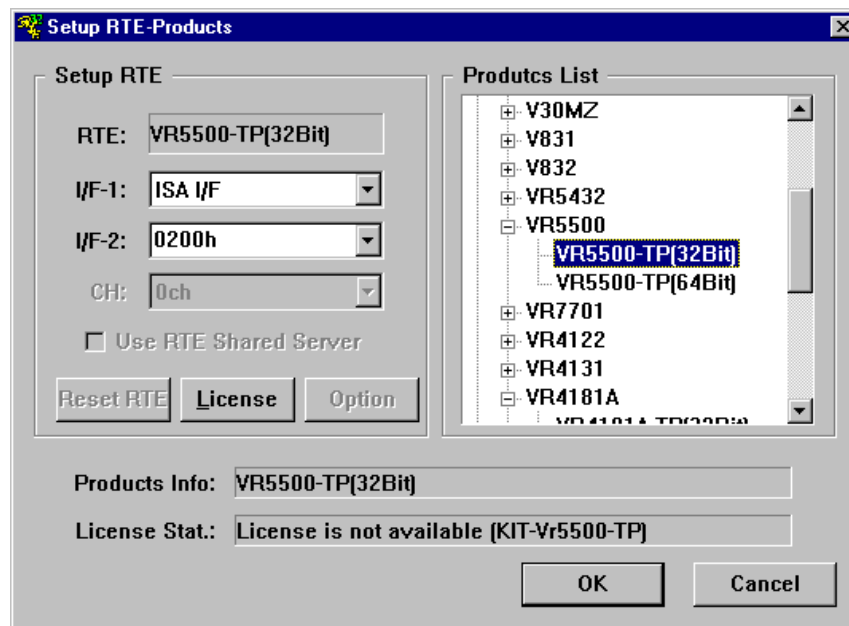
From Product List, select the VR5500-TP(xxx) located beneath the TP tree.

VR5500-TP(32Bit)   : Usually, please specify this.

VR5500-TP(64Bit)   : Please specify to do a register display by 64-Bit width
                            by MULTI.

<Selecting I/F-1, I/F-2>

Select and specify the host interface that suitable for your system from pull-down
menu. (The display in example shows that ISA Card is assigned)

<License>

Click the button to setup license checking with the license setup sheet attached to the
KIT package. For detail, please refer to the document of "RTE for WIN32".

<Function test>

If RTE for WIN32 is properly connected to the user system and capable of debugging, the following dialog box appears upon the normal completion of the function test. In this state, control from the debugger is possible.

If an error occurs during the test, the N-Wire cable is not properly connected. Check its connection.

> **Perform the ChkRTE2.exe function test after the RTE-xxxx-TP has been connected to the user system and the power to all the devices has been turned on.**

4. INITIALIZATION COMMANDS

Before debugging can be started, system initialization is required.

The following commands are available for system initialization, be sure to setup correctly before start to use the system.

To use Multi

Use following commands in Target window.

ENV command
   * Setup port mask
   * Specify JTAG clock
   * Others
ROM command
   * Specify ROM emulation condition
NC/NCD command
   * Specify data cache area for debugger software
NSPB/NSPBD command
   * Specify forbid software break area
NROM/NROMD command
   * Specify forced user area in rom emulation mapping area by ROM commad

To use PARTNER

Use following dialog.

Set CPU Environ dialog
   * Setup port mask
   * Specify JTAG clock
   * Others
Set Emulation ROM dialog
   * Specify ROM emulation condition
NC/NCD command
   * Specify data cache area for debugger software
NSPB/NSPBD command
   * Specify forbid software break area
NROM/NROMD command
   * Specify forced user area in rom emulation mapping area by ROM commad

5. . INTERFACE SPECIFICATIONS: CONVENTIONAL TYPE (KEL)

The signal connections of the conventional type (KEL) JTAG/N-Wire interface are listed below.

> **Use of the high-speed interface explained in the next chapter is recommended for new designing.**

Pin arrangement table

Pin number	Signal name	Input/output (user side)	Treatment (user side)
A1	CLKOUT	Output	22 - 33 Ω series resistor (recommended)
A2	TRCDATA0	Output	22 - 33 Ω series resistor (recommended)
A3	TRCDATA1	Output	22 - 33 Ω series resistor (recommended)
A4	TRCDATA2	Output	22 - 33 Ω series resistor (recommended)
A5	TRCDATA3	Output	22 - 33 Ω series resistor (recommended)
A6	TRCEND	Output	22 - 33 Ω series resistor (recommended)
A7	DDI	Input	4.7k - 10 kΩ pullup
A8	DCK	Input	4.7k - 10 kΩ pullup
A9	DMS	Input	4.7k - 10 kΩ pullup
A10	DDO	Output	22 - 33 Ω series resistor (recommended)
A11	DRST-	Input	4.7k - 50 kΩ pulldown
A12	Rmode*/ BkTGIO*	Input/Output	4.7k - 10 kΩ pullup
A13	NC.	------	Open

Pin number	Signal name	Input/output (user side)	Treatment (user side)
B1-B10	GND	------	Connection to the power GND
B11	NC.	------	Open
B12	NC.	------	Open
B13	+3.3V	------	Connection to the power

I/O (user side) indicates the input/output direction at the user board side.

A11: Open or It connects ColdReset* via an external circuit with VR5500 ES1.1. This signal is negative logic.

B13: Directly connect a power supply for I/O of the device that is to interface with the corresponding signal.

> **For details of the connectors and wiring, refer to the manual of RTE-XXXX-TP.**

6. INTERFACE SPECIFICATIONS: HIGH-SPEED TYPE (MICTOR)

The signal connections of the high-speed (MICTOR) JTAG/N-Wire interface are listed below.

> ⚠ **This interface is supported by RTE-2000-TP only.**

Signal connection list

Pin number	Connected signal name	Input/output (user side)	Treatment (user side)
1	GND		Connection to the GND
3(A8)	DCK	Input	4.7 k - 10 kΩ pullup
5(A9)	DMS	Input	4.7 k - 10 kΩ pullup
7(A7)	DDI	Input	4.7 k - 10 kΩ pullup
9(A10)	DDO	Output	22 - 33 Ω series resistor (recommended)
11	---	---	Open
13	---	---	Open
15	---	---	Open
17(A1)	TRCCLK	Output	22 - 33 Ω series resistor (recommended)
19(A6)	TRCEND	Output	22 - 33 Ω series resistor (recommended)
21(A2)	TRCDATA0	Output	22 - 33 Ω series resistor (recommended)
23(A3)	TRCDATA1	Output	22 - 33 Ω series resistor (recommended)
25(A4)	TRCDATA2	Output	22 - 33 Ω series resistor (recommended)
27(A5)	TRCDATA3	Output	22 - 33 Ω series resistor (recommended)
29	---	---	Open or Connection to the GND
31	---	---	Open or Connection to the GND
33	---	---	Open or Connection to the GND
35	---	---	Open or Connection to the GND
37	GND		Connection to the GND

Pin number	Connected signal name	Input/output (user side)	Treatment (user side)
2	GND		Connection to the GND
4(B13)	VCCIO	---	Connection to the I/O power supply of CPU (for power monitoring)
6(A11)	DRST-	Input	4.7 k - 50 kΩ pulldown
8(A12)	Rmode*/BkTGIO*	Input	4.7 k - 10 kΩ pullup
10(A13)	---	---	Open
12	---	---	Open
14(B11)	---	---	Open
16(B12)	---	---	Open
18	---	---	Open
20	---	---	Open
22	---	---	Open or Connection to the GND
24	---	---	Open or Connection to the GND
26	---	---	Open or Connection to the GND
28	---	---	Open or Connection to the GND
30	---	---	Open or Connection to the GND
32	---	---	Open or Connection to the GND
34	---	---	Open or Connection to the GND
36	---	---	Open or Connection to the GND
38	GND	---	Connection to the GND

Remark: ( ) indicates an equivalent pin of the KEL type connector.

I/O (user side) indicates the input/output direction at the user board side.

6-pin: Open or It connects ColdReset* via an external circuit with VR5500 ES1.1.
This signal is negative logic.

4-pin: Directly connect a power supply for I/O of the device that is to interface with the corresponding signal.

7. PRECAUTIONS

This chapter provides precautionary information on the use of KIT-VR5500-TP.

Precautions related to operation

1) Do not turn on the power to the user system while the power to KIT-VR5500-TP is off. Doing so can cause a malfunction.
2) KIT-VR5500-TP externally controls the debugging control circuit built into the CPU Consequently, KIT-VR5500-TP does not operate correctly unless the following conditions are satisfied:
   * KIT-VR5500-TP is properly connected to the user system using the N-Wire cable.
   * The power to the user system is on so that the CPU can run correctly.

Precautions related to functions

1) This KIT corresponds to a 32-bit address space. It does not correspond to the address mode of 64-Bit.
2) A virtual address corresponds, only when TLB is in the state of always hitting statically.
3) It is related with real-time trace.
   * The disassemble display of real-time trace is performed by reading the contents of a memory on the basis of the branch information from CPU. Therefore, when the contents of a memory are changed after execution, the right execution history cannot be displayed. Moreover, when an error is in branch information, an analysis display cannot be done correctly.
   * When it runs from a break point and using hardware break point one instruction of an execution start address does not write into trace.
   * Trace is automatically ended on condition that the following.
      - When the trigger point was passed and a break is taken.
      - When a break is taken in the state of the delay mode.
4) Don't LOCK cache. When it LOCKs, neither break in the area, nor step execution and rewriting of a memory can be performed normally.
5) For further information, be sure to refer to the Release Note of the KIT.
6) The following is the limitation in the case of doing ICE of VR5500 ES1.1.
   * The section about N-Wire in the limitation document of NEC Corp. issue corresponds to the limitation at the time of ICE use. Please use it after confirmation.
   * When trace is done from immediately after execution , a packet unnecessary one line is displayed just before execution. This should be disregarded. It is the line of the following (a).

   ```
   Cycle     Sub  Address    Code       Instruction     EXT      Stat
   +000001   ---- --------   --------   1  Count        1111     NSEQ    << (a)
   +000004   ---- bfc00000   0bf00100   j  bfc00400     1111     TPC
   +00000f   ---- bfc00004   00000000   nop             1111     NSEQ
   +000012   ---- bfc00400   40806800   mtc0  r0,$13     1111     NSEQ
   ```
7) CPU will leave control of ICE in the following cases, and VR5500/VR5500A will start execution freely. When you become such a situation, please reboot a debugger, or operate an initialization command (when using an internal command, they are the init command or the reset command), and resume debugging from the start.
   * When a user system is repowered on
   * When cold reset is applied from on a user system to CPU

8)   Please connect EXT connector :A4 pin (RESETOUT# signal) of RTE-2000-TP to the reset circuit on a user system to reset the whole user system by the initialization command from ICE. To use this function, rte4win32 needs to be newer than 5.13B14 or 5.13.00, and it.