KIT-V850E/ME2-TP(-H)

User's Manual (Rev.1.00)

RealTimeEvaluator

Software Version Up

* The latest RTE for Win32 (Rte4win32) can be down-loaded from following URL.
  http://www.midas.co.jp/products/download/english/program/rte4win_32.htm

Notice

Trademarks

REVISION HISTORY

Rev.1.00	Apr., 12, 2006	1st edition in English - RTE-2000H-TP supported

CONTENTS

1. OVERVIEW

KIT-V850E/ME2-TP(-H) is the software that performs in-circuit emulation for systems that have NEC RISC micro processor V850E/ME2 for debugging purposes. The match of the hardware which can be used, and KIT is as follows.

- KIT-V850E/ME2-TP : It is KIT for RTE-2000-TP.
- KIT- V850E/ME2-TP-H : It is KIT for RTE-2000H-TP.

The description method in this manual is described below.

When KIT- V850E/ME2-TP and KIT- V850E/ME2-TP-H are not distinguished, these KITs are described to be KIT-xxxx-TP (-H).

And, hardware is described to be RTE-2000(H)-TP by explanation which does not distinguish RTE-2000-TP and RTE-2000H-TP.

Thus on using the product, please refer to the **RTE-XXXX-TP Hardware User's Manual** also, that is main part of whole debugging system.

This product comes with the following components. First check that none of the components are missing.

- RTE for Win32 (Rte4win32) Setup Disk
- User's manual (This manual)
- License sheet

2. HARDWARE SPECIFICATIONS

Emulation

Target device			V850E/ME2	
RTE-TP type to be used			RTE-2000-TP	RTE-2000H-TP
JTAG-IF cable (() Inside is an option.)			RTE-NEC/MICTOR38-2K	PN-JTAG-N-A36(72/144)
Emulation functions				
	CPU operating frequency		Not limited (*5)	
	Interface		JTAG/N-Wire	
	Operation voltage		1.8 - 3.3 V(5V tolerant) (*2)	1.2 - 3.3 V(5V tolerant)
	JTAG clk		100 kHz - 25 MHz	
Event function				
	Number of events			
		Setting of execution address	8	
		Setting of data access	4	
		Address specification	Maskable	
		Data specification	Maskable	
		Status specification	Maskable	
		Number of sequential unit stages	4	
		Pass Counter	12-bit	
Break functions				
	Hardware break points			
		Setting of execution and Data access	2	
		Address specification	Maskable	
		Data specification	Maskable	
		Status specification	Maskable	
	Software break points		100	
	Breaks that can be set using events		Supported	
	Step breaks		Supported	
	Manual breaks		Supported	
	External breaks (High/Low edge)		Supported	
Trace functions				
	Trace data bus		4 bits	
	Trace memory (() Inside is an option.)		4 bits ×256k words	4 bits × 1M(2M/4M) words
	Trace setting		Supported	
		execution address	Supported	
		data access	Supported	
		event	Supported	
		external input	Supported	
	Start/stop by execution address		Supported	
	Trace delay (() Inside is an option.)		0 - 3FFFF	0 – FFFFF(1FFFFF/3FFFFF)
	Trace clock (() Inside is an option.)		max133 MHz	max333MHz(B spec.=400MHz)
	Time tag		100 ns - 30 h	
	Disassembled trace data display function		Provided	
	Complete trace mode specification function (no real time)		Provided	
ROM emulation functions (*4)				
	Map function in block (USER/EMEM)		64k words	
	Used as RAM		Supported	
	Memory capacity		8M - 128M bytes	
	Access time (():burst cycle)		35 ns (30 ns) (*1)	
	Operation voltage		1.8 - 5 V (*2)	
	Electrical condition		LV-TTL, 5V tolerant (*3)	
	Number of ROMs that can be emulated			
		DIP-32pin-ROM (8-bit ROM)	4 (max.)	
		DIP-40/42pin-ROM (16-bit ROM)	4 (max.)	
		Extend STD-16BIT-ROM connector	4 (max.)	
	Sizes of ROMs that can be emulated (bits)			
		DIP-32-ROM (8-bit bus)	1M, 2M, 4M, 8M (27C010/020/040/080)	

		DIP-40-ROM (16-bit bus)	1M, 2M, 4M (27C1024/2048/4096)	
		DIP-42-ROM (16-bit bus)	8M, 16M (27C8000/16000)	
		Extend STD-16BIT-ROM (16-bit bus)	1M, 2M, 4M, 8M, 16M, 32M, 64M, 128M, 256M (32M bytes)	
	Bus width specification (bits)		8/16/32	
High speed down load function			None	Supported (*6)
Pin mask functions			RESET, STOP, NMIx, HLDRQ	

*1, 2, 3: Values when RTE-2000(H)-TP + CBL-STD16-2K is used.

*2: Note that the DC characteristics of each cable may not electrically match when the supply voltage is 2.3 V or less.

*4: Up to four E.MEM boards can be mounted to RTE-2000(H)-TP, and the maximum capacity is 128M bytes. Two E.MEM boards are necessary for the 32-bit width, and four are necessary for the 64-bit width. One board is necessary per ROM with an 8-bit bus width.

*5. Please contact us, if you use it below 100kHz.

*6. Using a high-speed download function, PB-HSDL-xx of an option is necessary. Please confirm each support situation in KIT separately.

3. RTE for WIN32

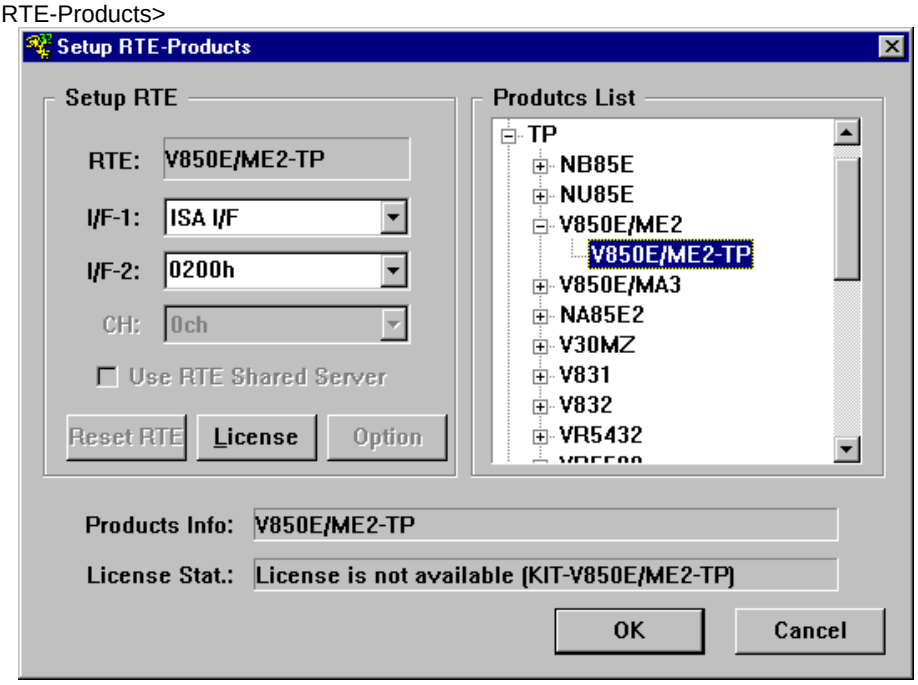
This chapter describes the setting of RTE for WIN32.

Invoking ChkRTE2.exe

After finishing to connect to the user system and apply the power supply for all equipments, invoke ChkRTE2.exe to set up the configuration of "RTE for WIN32".

Please set up the "RTE for WIN32" configuration at least one time for newly installed hardware.

<Setup RTE-Products>



<Selecting RTE>

From Product List, select the V850E/ME2-TP located beneath the TP .

<Selecting I/F-1, I/F-2>

Select and specify the host interface that suitable for your system from pull-down menu. (The display in example shows that USB-IF is selected.)

<License>

Click the button to set up license checking with the license setup sheet attached to the KIT package. For details, please refer to the manual of "RTE for WIN32".

When you use it by RTE-2000H-TP, please use rte4win32 ver.6.00.xx or later.

<Function test>

If RTE for WIN32 is properly connected to the user system and capable of debugging, the following dialog box appears upon the normal completion of the function test. In this state, control from the debugger is possible.

If an error occurs during the test, the user system has a failure or the JTAG-IF cable is not properly connected. Check its connection.

Perform the ChkRTE2.exe function test after the RTE-xxxx-TP has been connected to the user system and the power to all the devices has been turned on.

4. INITIALIZATION COMMANDS

Before debugging can be started, system initialization is required, depending on hardware of the user system.

The following commands are available for system initialization. Be sure to set up correctly before start to use the system.

To use Multi

Use the following commands in Target window.

ENV command
* Specify pin mask.
* Specify JTAG clock.
* Others

ROM command
* Specify ROM emulation condition.

NC/NCD command
* Specify data cache area for debugger.

NSPB/NSPBD command
* Specify forbid software break area.

NROM/NROMD command
* Specify forced user area.

To use PARTNER

Use the following dialog boxes and commands.

CPU Environ dialog
* Specify pin mask.
* Specify JTAG clock.
* Others

Emulation ROM dialog
* Specify ROM emulation condition.

NC/NCD command
* Specify data cache area for debugger.

NSPB/NSPBD command
* Specify forbid software break area.

NROM/NROMD command
* Specify forced user area.

When you change the IIRAM_CHK parameter of the ENV command, please attach "&" and use an internal command. (&env …)
It is not usually necessary to change this parameter.

5. INTERFACE SPECIFICATIONS: CONVENTIONAL TYPE (KEL)

The signal connections of the conventional type (KEL) JTAG/N-Wire interface are listed below.

Use of the high-speed interface explained in the next chapter is recommended for new designing.

Signal connection list

Pin number	Connected signal name	Input/output (user side)	Treatment (user side)
A1	TRCCLK	Output	22 - 33 Ω series resistor (recommended)
A2	TRCDATA0	Output	22 - 33 Ω series resistor (recommended)
A3	TRCDATA1	Output	22 - 33 Ω series resistor (recommended)
A4	TRCDATA2	Output	22 - 33 Ω series resistor (recommended)
A5	TRCDATA3	Output	22 - 33 Ω series resistor (recommended)
A6	TRCEND	Output	22 - 33 Ω series resistor (recommended)
A7	DDI	Input	4.7 k - 10 kΩ pullup
A8	DCK	Input	4.7 k - 10 kΩ pullup
A9	DMS	Input	4.7 k - 10 kΩ pullup
A10	DDO	Output	22 - 33 Ω series resistor (recommended)
A11	DRST-	Input	4.7 - 50 kΩ pulldown
A12	DBINT	Input	Open
A13	NC.	------	Open

Pin number	Connected signal name	Input/output (user side)	Treatment (user side)
B1-B10	GND	------	Connection to the GND
B11	NC.	------	Open
B12	NC.	------	Open
B13	VCCIO	------	Connection to the I/O power supply (+3.3 V normally)

I/O (user side): Input/output direction at the user board side

B13-VCCIO: Directly connect a power supply for I/O of the device that is to interface with the corresponding signal.

For details of the connectors and wiring, refer to the manual of RTE-XXXX-TP.

CBL-KEL26 of an option is necessary to use this connector by RTE-2000H-TP.

6. INTERFACE SPECIFICATIONS: HIGH-SPEED TYPE (MICTOR)

The signal connections of the high-speed (MICTOR) JTAG/N-Wire interface are listed below.

This interface is supported by RTE-2000(H)-TP only.

Signal connection list

Pin number	Connected signal name	Input/output (user side)	Treatment (user side)
1	GND		Connection to the GND
3(A8)	DCK	Input	4.7 k - 10 kΩ pullup or pulldown
5(A9)	DMS	Input	4.7 k - 10 kΩ pullup or pulldown
7(A7)	DDI	Input	4.7 k - 10 kΩ pullup or pulldown
9(A10)	DDO	Output	22 - 33 Ω series resistor (recommended)
11	---	---	Open
13	---	---	Open
15	---	---	Open
17(A1)	TRCCLK	Output	22 - 33 Ω series resistor (recommended)
19(A6)	TRCEND	Output	22 - 33 Ω series resistor (recommended)
21(A2)	TRCDATA0	Output	22 - 33 Ω series resistor (recommended)
23(A3)	TRCDATA1	Output	22 - 33 Ω series resistor (recommended)
25(A4)	TRCDATA2	Output	22 - 33 Ω series resistor (recommended)
27(A5)	TRCDATA3	Output	22 - 33 Ω series resistor (recommended)
29	---	---	Open or GND
31	---	---	Open or GND
33	---	---	Open or GND
35	---	---	Open or GND
37	GND		Connection to the GND

Pin number	Connected signal name	Input/output (user side)	Treatment (user side)
2	GND		Connection to the GND
4(B13)	VCCIO	---	Connection to the I/O power supply of CPU (for power monitoring)
6(A11)	DRST-	Input	4.7 k - 50 kΩ pulldown
8(A12)	DBINT	Input	Open
10(A13)	---	---	Open
12	---	---	Open
14(B11)	(EVTTRG)	Output	Open
16(B12)	---	---	Open
18	---	---	Open
20	---	---	Open
22	---	---	Open or GND
24	---	---	Open or GND
26	---	---	Open or GND
28	---	---	Open or GND
30	---	---	Open or GND
32	---	---	Open or GND
34	---	---	Open or GND
36	---	---	Open or GND
38	GND	---	Connection to the GND

Remark: ( ) indicates an equivalent pin of the KEL type connector.

I/O (user side) indicates the input/output direction at the user board side.

Pin 14 (EVTTRG) is unused.

7. PRECAUTIONS

This chapter provides precautionary information on the use of KIT-V850E/ME2-TP(-H).

Precautions related to operation

1) Do not turn on the power to the user system while the power to this system is off. Doing so can cause a malfunction.
2) This system externally controls the debugging control circuit (DCU) built into the CPU. Consequently, this system does not operate correctly unless the following conditions are satisfied:
   * This system is properly connected to the user system using the JTAG-IF cable.
   * The power to the user system is on so that the CPU can run correctly.
3) Please set up the break point to internal instruction RAM after transmitting a program. The break point set up before transmission is invalid.

Precautions related to functions

1) The PC Register is set to 0x100000H after Reset operation.
2) The memory access to the internal Instruction RAM is fixed to either Read or Write Only by the setting of the IRAMM Resister located at the address 0xFFFFF80AH. This feature introduces the following cautions.
   a) When the CPU fetches instructions from the internal RAM memory space, the Memory Access Mode needs to be Read Only Mode. In case that the CPU Execution Start Address is located within the internal RAM memory space, the Debug Control Software check the Memory Access Mode at first, and if the Memory Access Mode is set to Write Only as well as the IIRAM_CHK parameter which is set in the 'ENV command' is assigned to 'Enable (Default)', the Debug Control Software returns 'Error' before the CPU executes the program. In case that the 'Error' occurs, change the Memory Access Mode from Write Only to Read Only.
   b) When the memory access to the internal Instruction RAM memory space is operated by the Debug Control Software, both read or write memory access can be done regardless of the Memory Access Mode in the IRAMM register. This is because the Debug Control Software temporary changes the Memory Access Mode in the IRAMM register when accessing to the internal RAM memory space.
3) The disassembly display of real-time trace data is performed by reading the contents of memory at the point the trace display command is issued, according to the branching information received from the CPU. Consequently, the disassembly display of the program located in RAM of the user system is not correct if changes (including erroneous writing due to a CPU hang up) are made after program execution.
4) If the trace information is limited, trace display may not be correctly performed. Therefore, usually use the initial values (all traces are output).
5) A breakpoint in the ROM space is invalid if the breakpoint is set to the second instruction of an instruction string that simultaneously execute two instructions.
6) For the CPU implemented on-chip cache, it is not possible to debug correctly during the cache is locked. If the cache is locked, the capabilities such as break, step execution, or memory modification for corresponding memory region might malfunction.
7) If the release note etc. is appended, be sure to refer to them.

The cautions in the case of connecting with V850E/ME2-ES1
The lock flag (LOCKR:LOCK) of PLL is not set to "0" at the time of ICE.
If the external WAIT- has LOW level at the time of access to internal instruction RAM, the control from ICE will become impossible.

8. DETAILS OF TRACE FUNCTIONS

This appendix describes the real-time trace function.

Overview of the trace function

The function of real-time trace is the following.

- The execution information (trace data) outputted from CPU is written in the trace buffer of ICE.
- An execution history is shown as a "trace" command based on the trace data in this trace buffer.

You can set the trace mode, trace start condition, trigger condition, section condition, qualify condition, and other conditions to specify the loading of trace data.

For the flow of loading trace data, see Figures 1 and 2.

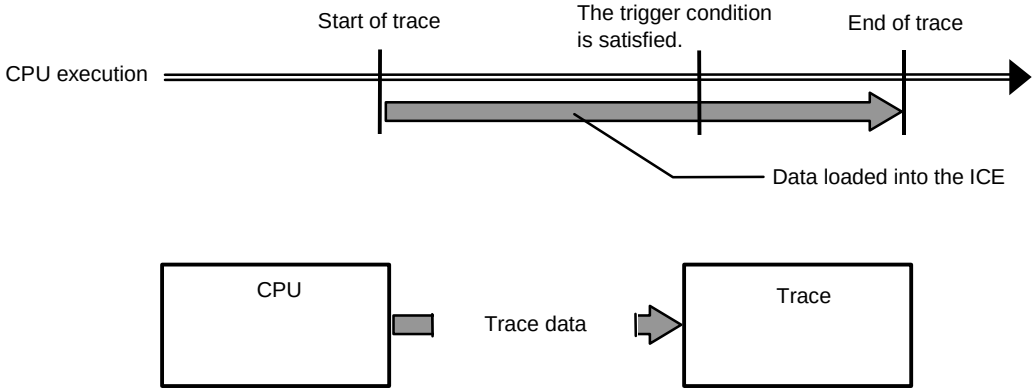


Figure 1 Flow of loading trace data

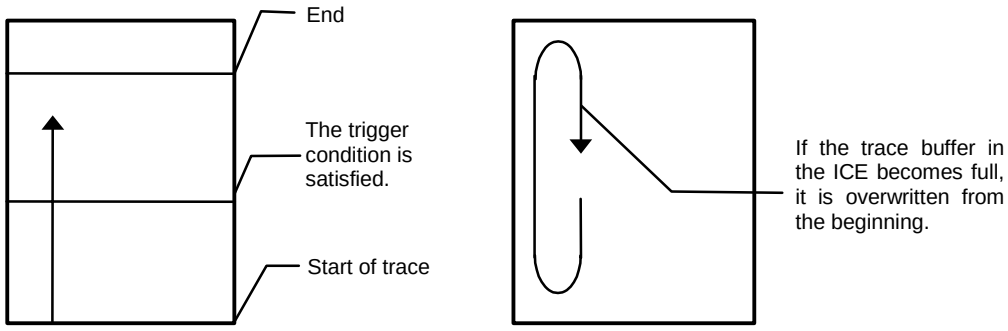


Figure 2 Trace data in the ICE

Delay count

The delay count means the number of cycles in which trace data is to be loaded after the trigger condition is satisfied (Figure 3). The number of cycles differs depending on the type of CPU execution. One cycle is not one execution unit.

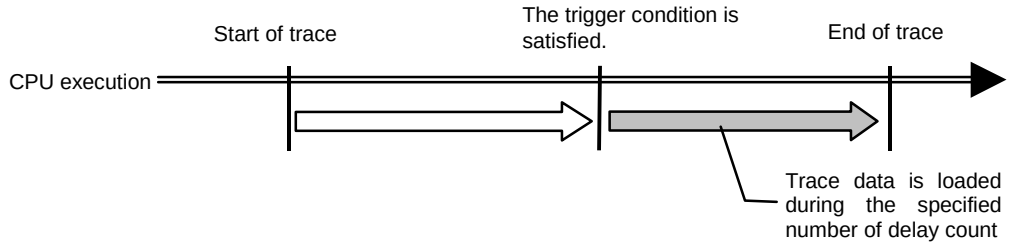


Figure 3 Flow of delay count

Trace execution mode

In **the real-time mode**, trace data is loaded with priority given to the CPU execution. If the trace buffer (FIFO) in the CPU becomes full, part of trace data may not be loaded (Figure 4).

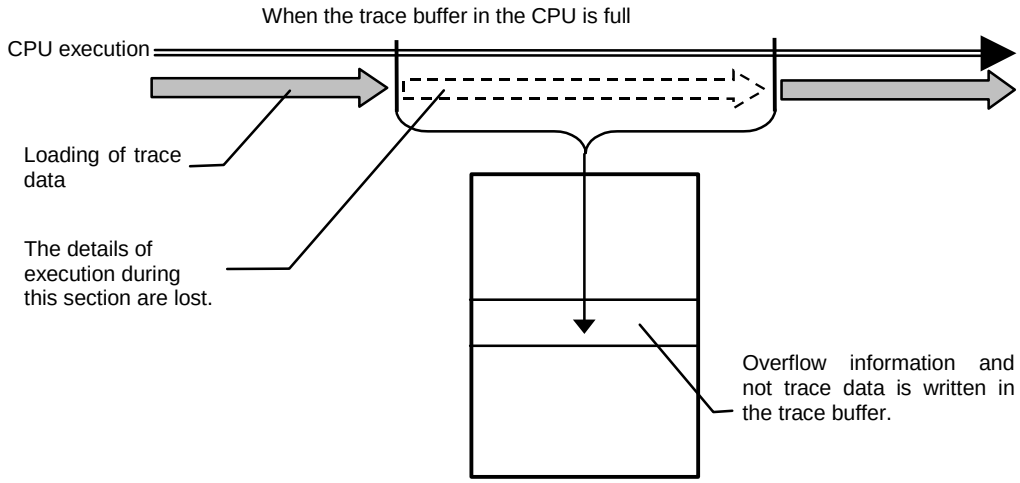


Figure 4 Real-time mode

In **the non-real-time mode**, all trace data can be loaded. If the trace buffer (FIFO) in the CPU becomes full in this mode, the CPU execution is temporarily stopped and is automatically restarted (Figure 5).

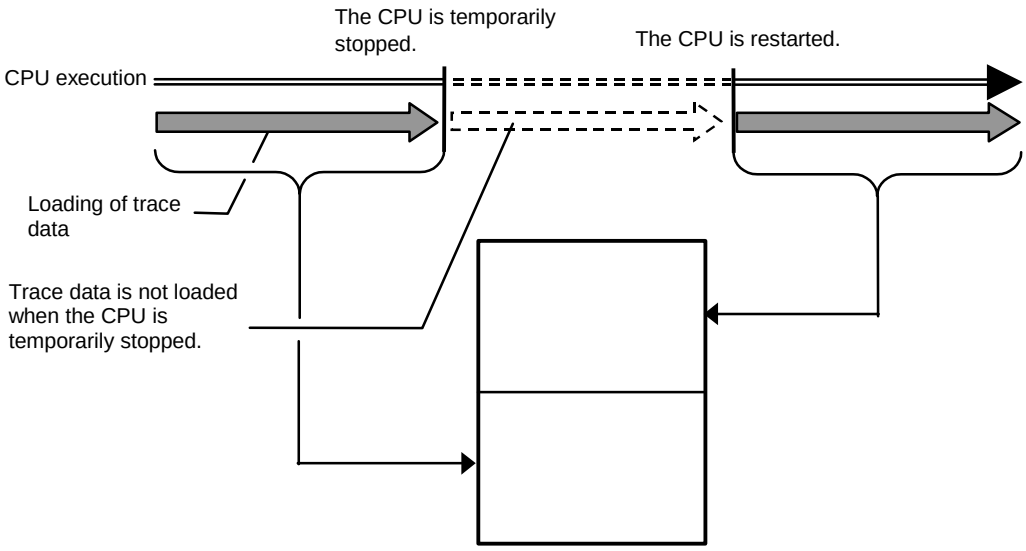


Figure 5 Non-real-time mode

Starting trace

To start loading trace data, the following methods are available (Figure 6)

In order to use trace switch point 1 for a start condition, "tr1_all" needs to be set up of the tron command.

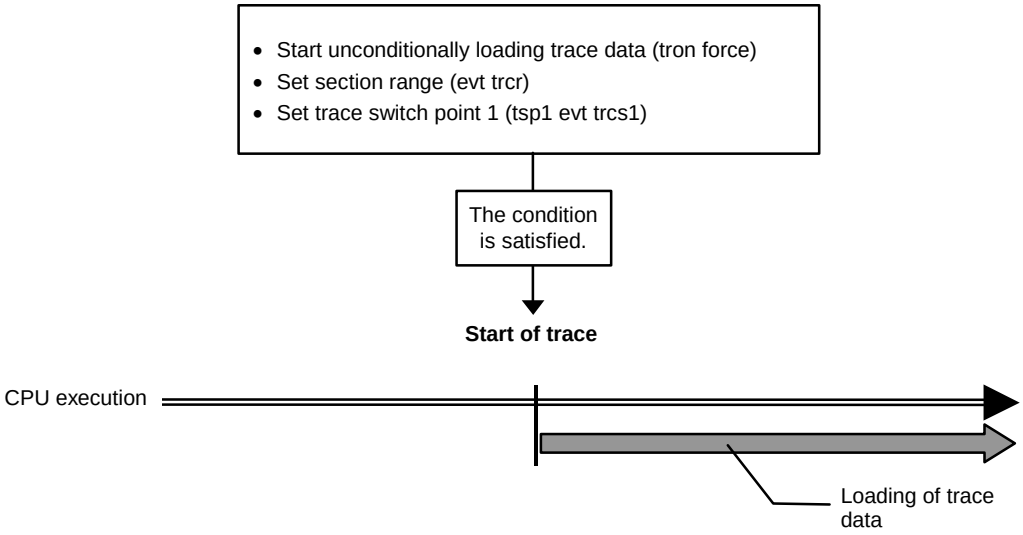


Figure 6 Starting trace

Trigger condition

A trigger condition is used as the start point of delay count (Figure 7). You can set a trigger condition to check the details of the execution before and after the trigger.

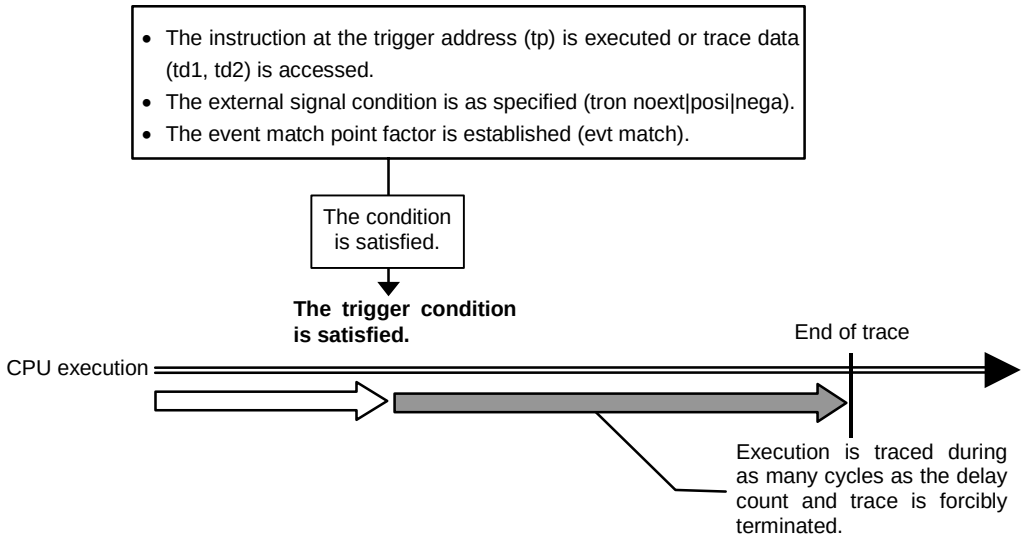


Figure 7 Trigger condition

Stopping trace

To stop loading trace data, the following methods are available.(Figure 8)

In order to use trace switch point 2 for a stop condition, "tr2_" needs to be set up of the tron command.

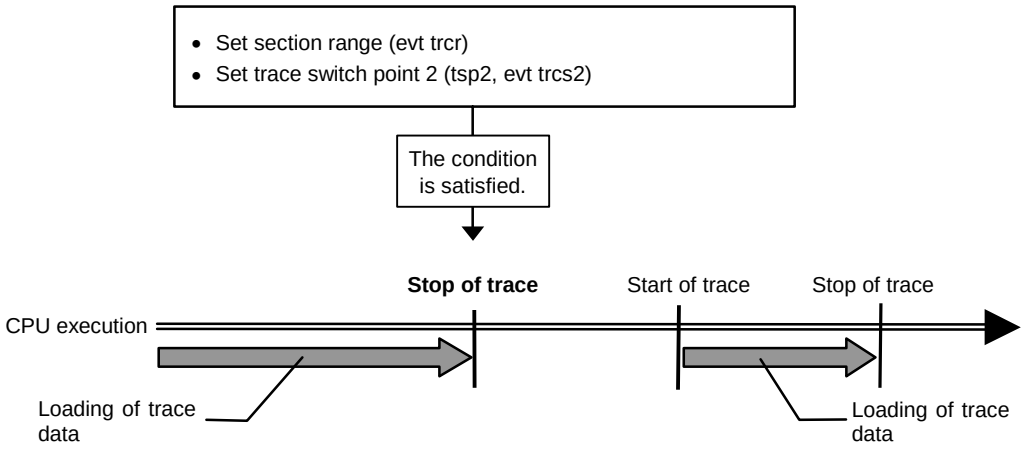


Figure 8 Stopping trace

Terminating trace

After trace is terminated, no more trace data is loaded.(Figure 9).

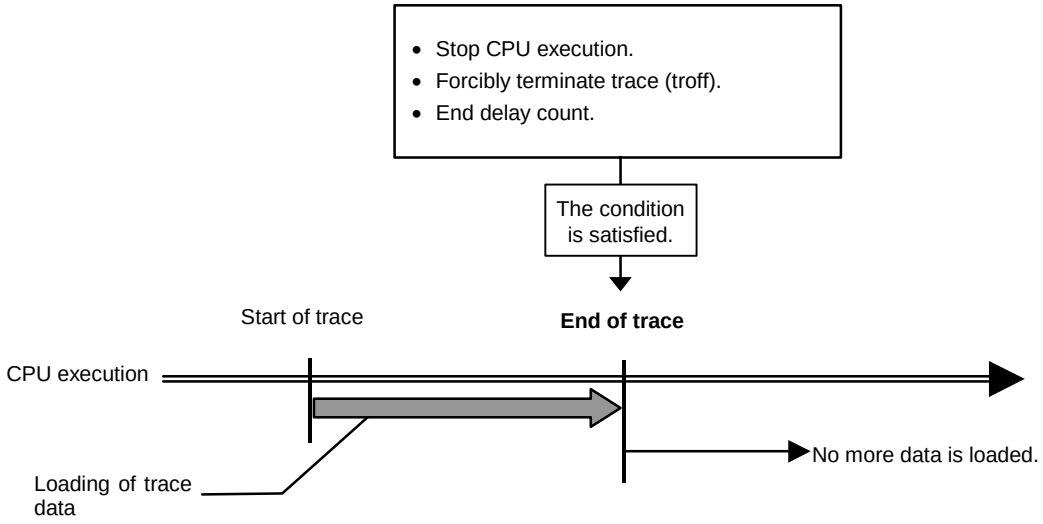


Figure 9 Terminating trace

Forced delay mode

In the forced delay mode, trace is forcibly terminated when trace data is loaded during the specified delay count (number of cycles) after the start of trace. In this mode, the trigger condition is ignored (Figure 10). When CPU execution starts, trace is started in this mode.

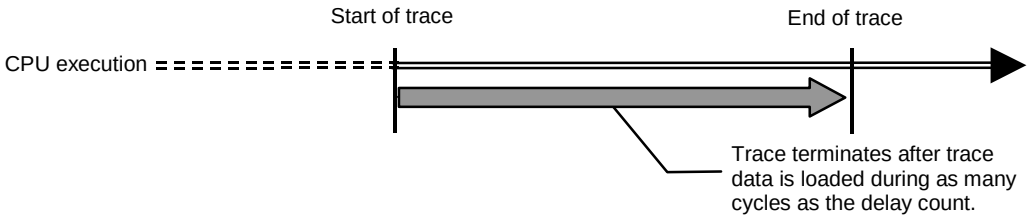


Figure 10 Forced delay mode